Electronics Technology File

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ABSTRACT: The Electronics Technology File (ETF) defines the preferred set of components and design rules from the chip edge through the backplane interconnect levels. Access VTX TECHFILES to obtain the most current information regarding these tech files.

APPLICABILITY: The ETF is a tool that aids concurrent engineering by providing a document framework between product design and manufacturing specialists.

STATUS: APPROVED 30-Dec-1992; use VTX SMC for current status.

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Preface

Rev 4.1 of the Electronics Technology File document is the second releases of this document. It is expected that Rev 4.1 will be used in lieu of DEC STD 030-4 Printed-Wiring Board Design Requirements and DEC STD 030-5 Module Assembly and Component Insertion Rules. The chapter release schedule is as follows:

Rev 4.0 June 1992

Chapter 1 - Introduction
Chapter 2 - Principles for Design Optimization
Chapter 6 - Printed-Wiring Boards
Chapter 7 - Module Layout Design Requirements

Rev 4.1 December 1992

Chapter 3 - IC Packaging
Chapter 4 - Non-IC Components
Chapter 5 - Connectors
Chapter 9 - Product Data
Chapter 11 - Module Electrical Design

EL-MF787-00 - Corporate Electronics - Packaging and Interconnect Strategy

Rev 4.2 March 1993

Chapter 8 - Backpanels and Backplane Assemblies
Chapter 10 - Module Cost and Quality Estimation
Chapter 12 - Thermal Design
Chapter 13 - Reliability Considerations
Chapter 14 - Design and Product Verification

Appendix A - Module Assembly and Test Process
Appendix B - Preferred LSI/VLSI Components
Appendix C - Module CAD/CAE Tools

Send comments or change requests to:

Techfiles, MLO5-3/B97, KELVIN::TECHFILES or TECHFILES@KELVIN@VMSMAIL

Chapter 1: Introduction

1.1 Overview

The Electronics Technology File (ETF) simplifies and accelerates the design, manufacturing ramp, and time-to-profit of electronics modules while lowering the overall cost of the product realization process. It is not a one-for-one replacement for Digital's standards system (although the ETF does supersede DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements and DEC STD 030-5 Module Manufacturing Standard - Module Assembly and Component Insertion Rules); instead, the ETF is a tool that aids concurrent design by providing a discussion framework between product design and manufacturing specialists. The ETF's goal is to streamline and decentralize the decision process while ensuring substantial uniformity in design style and overall design commonality across the Corporation. The ETF is expressly intended to foster standardization in all areas that do not lead to perceivable advantages for the end customer while allowing flexibility instead of rigid standards.

The ETF provides three major sets of information to product designers:

- preferred components and associated design rule
- design guidelines and best-practice recommendations
- detailed design data

Use of the preferred components and adherence to a minimum set of design rules ensures consistency with standard Digital manufacturing processes and results in predictability in performance, cost, quality, and product ramp. The design guidelines and data sections provide most of the data and techniques required for module physical design. Each section provides appropriate pointers to sources of more detailed information.

The intended users of the ETF are the members of the concurrent engineering team: design technologists, design engineers, design services specialists, and manufacturing engineers.

The ETF will be updated and published on a quarterly basis, and will be synchronized with the Electronics Packaging Working Group (EPWG) technology introduction strategy and new process capabilities as they are introduced. EL-MF787-00, Corporate Electronics - Packaging and Interconnect Strategy, provides a summary of the EPWG strategy.

1.2 Scope

The ETF scope extends from the chip edge through the backplane interconnect levels and is focused on the physical design of electronic modules. Design with analog components is covered except for application-specific design rules and features; power modules are NOT included.

The ETF can be used in the design of a variety of electronics modules:

- Performance-driven design
- Cost-driven designs
- Density or size-driven designs
- Backplanes

1.3 Module Design Committee

The ETF is controlled by a cross-organizational Module Design Committee (MDC) that maintains review and approval responsibility for the document. The publication and revision procedure is outlined in Section 1.5.

The current composition of the MDC follows (use VTX ELF for telephone numbers).

Member	Affiliation	Electronic Mail Node
Al Austin	ASO Manufacturing	DNEAST::AUSTIN_AL
Dennis Brown	Storage (disks/tapes)	LEDS::BROWNDEN
Dan Callahan	VSS/DCSS	WONDER::CALLAHAN
Dave Conroy	SCO	AD::CONROY
Jeff Copeland	PCSP/VIPS	ROYALT::COPELAND
Jon Crowell	VSS/ESB	DIODE::CROWELL
John Cyr	NaC	NAC::CYR
Mike Elia	MTTS	WEDOIT::ELIA
Larry Fahey	MTTS	GIAMEM::FAHEY
Les Fox	TDA	CARROL::FOX
Rob Hannemann (Chair)	Technology	KELVIN::HANNEMANN
Wayne Parker	SCO/SEG	ORACLE::PARKER
Charles Schnare	Storage (subsystems)	SUBSYS::SCHNARE
Reinhard Schumann	USS/WSE	MAST::SCHUMANN
Paul Vilcans	TDA	KELVIN::VILCANS
Debbie Vogt	USS/WSE	WRKSYS::VOGT

The production and revision of ETF chapters is the responsibility of a subcommittee of the MDC consisting of Chapter Captains for each chapter or appendix. These chapter captains are expected to assemble cross-organizational technical working groups to provide guidance, critique, and data for their ETF chapters. Chapter captains may be replaced by nomination of a successor by the resigning captain and subsequent approval by the MDC.

The current chapter captain roster follows:

Chapter Name	Chapter Captain	Electronic Mail Node
Techfile Project Manager	P. Vilcans	KELVIN::VILCANS
1.0 Introduction	R. Hannemann	KELVIN::HANNEMANN
2.0 Principles for Design Optimization	J. Mavroides	KELVIN::MAVROIDES
3.0 IC Packaging	S. Hansen	KELVIN::HANSEN
4.0 Non-IC Components	D. Brouillet	GOLF::BROUILLET
5.0 Connectors	S. Daughtrey	POLAR::DAUGHTREY
6.0 Printed-Wiring Boards	G. Gagnon	BOARDS::GAGNON
7.0 Module Layout Design Requirements	J. Mavroides	KELVIN::MAVROIDES
8.0 Backpanels and Backplane Assemblies	A. Knaut	POLAR::KNAUT
9.0 Product Data	H. Loken	VSSCAD::LOKEN
10.0 Module Cost and Quality Estimation	J. Mavroides	KELVIN::MAVROIDES
11.0 Module Electrical Design	R. Evans	CARROL::EVANS
12.0 Thermal Design	E. Allen	KELVIN::ALLEN
13.0 Reliability Considerations	C. Davidson	KELVIN::DAVIDSON
14.0 Design and Product Verification	M. Roche	CARROL::ROCHE
Appendices		
A. Module Assembly and Test Process	C. Becker	MACNAS::CBECKER
B. Preferred LSI/VLSI Components	B.Brownell	MILKWY::BROWNELL
C. Module CAD/CAE Tools	H. Wong	CARROL::WONG
EPWG Strategy	S. Hansen	KELVIN::HANSEN

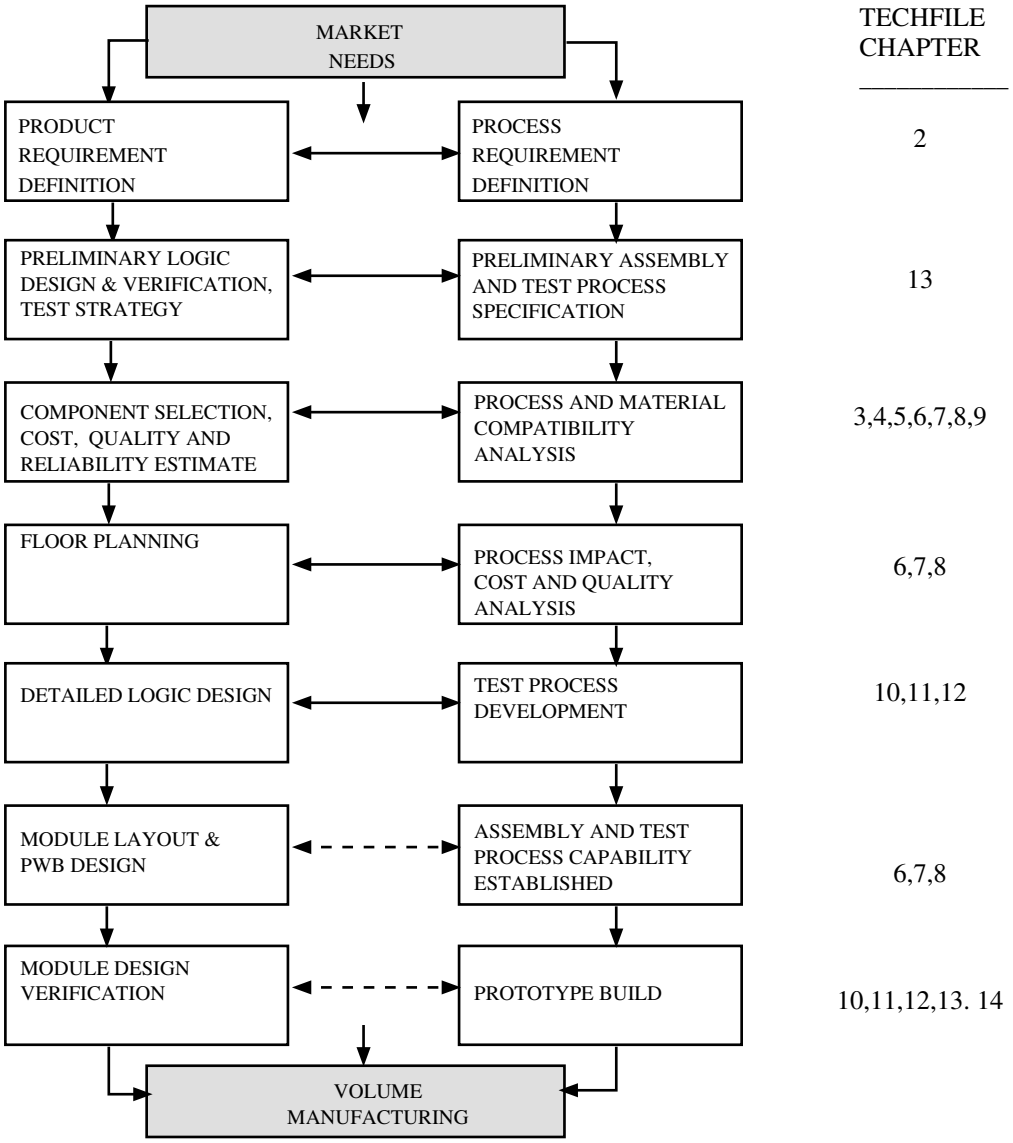
1.4 ETF Structure

The ETF has three main pats:

- **Part 1** provides a short description of preferred component choices and design practices.
- **Part 2**, consisting of Chapters 6, 7, and 8, presents a minimum set of layout and design rules to ensure maximum compatibility with the modules manufacturing process.
- **Part 3** provides a standalone tutorial on best-practice design across a spectrum of technology disciplines.

The chapter structure is arranged to be consistent with the normal concurrent design flow, as shown in Figure 1-1 below:

Figure 1-1: Concurrent Engineering Model for Techfiles



1.5 Publication and Revision Procedure

After initial publication, the ETF will be updated and issued quarterly. The revision numbering scheme will be of the form Rev *x.m* where *x* is the current EPWG-defined technology platform and *m* is the quarterly revision number.

ETF Distribution will be by hardcopy to a controlled circulation list and will also be available in electronic format from Standards and Methods Control.

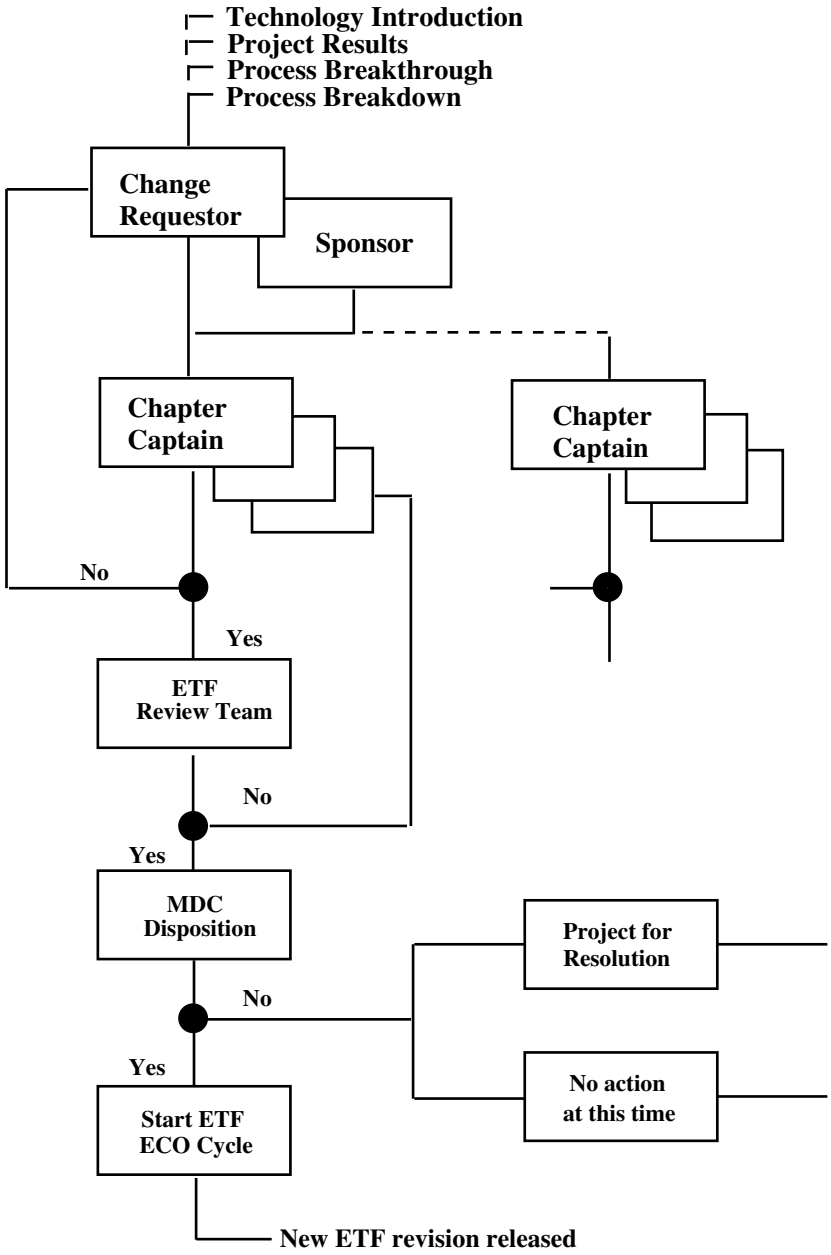
Publication and amendment of the ETF is the responsibility of the MDC. Changes to the ETF will be recommended by the appropriate chapter captain and considered in depth by the MDC. On approval, changes will be implemented in the next quarterly revision.

1.6 ETF Content Change Procedure

Figure 1-2 illustrates the process for requesting a change to the ETF document

Figure 1-2: ETF Change Process

.



1.6.1 Definitions and Responsibilities

Change Requestor: Anyone in Design, Manufacturing or Engineering who has a specific change, addition, or deletion that they would like implemented in the ETF. The requestor is responsible for providing the data (technical and financial) to the appropriate chapter captain that supports the change request. The requestor will use the Change Request Form (see Figure 1-3).

Sponsor: The sponsor is a member of the ETF Chapter Review Team. The use of a sponsor is optional. The sponsor will assist the requestor in completing the Change Request Form, and will also help him/her in understanding the current content of the ETF.

Chapter Captain: The chapter captain is responsible for the content of the ETF chapter. All change requests go directly to the chapter captain . A copy of all changes should also be sent to KELVIN::TECHFILES for tracking purposes. The chapter captain meets with or contacts the requestor for further explanation of suggested changes or other necessary information.
The chapter captain has an advisory committee (in addition to the ETF Chapter Review Team) that he or she may call upon for technical support.

ETF Chapter Review Team: The review team consists of manufacturing, design, or technology specialists who will be able to evaluate the data presented with each change request and "speak" for their organization in approving or rejecting changes.

Each chapter will have a different set of team members. The review team members for each chapter is documented in each chapter.

MDC: The Module Design Committee (MDC) is responsible for final approval of the changes.

1.6.2 Change Policies and Time Requirements

Each chapter captain will have a review team identified by December 1992.

The review team will perform its tasks electronically when possible.

The chapter captain review will have a two week time limit.

The review team review will have a two week time limit.

Each change request should be closed within four weeks. Exceptions to this are major technology introductions or other items that require that the team meet. Review teams will meet at least twice a year , more often if necessary or feasible.

If a change request is rejected at any level, the chapter captain is responsible for issuing a clear response to the requestor describing why the change request was rejected.

1.7 Change Request Form

PROPOSED TO TECHFILE

Date of Proposal:	**Committee action date:**
Submittor:	**Action Requested:**
DTN: **Mailstop:**	
ENET:	

Electronic Technology File: **Rev:**

Section: **Rev:** **Page:** **Paragraph:**

Current text:

Proposed text:

Justification, References (Technical and Financial):

Impact to present section:

Impact to other sections:

Reviewer's Comments:

Committee Action:

1.8 A Note on Metric Dimensioning

A variety of standard electronic components are dimensioned using English units, while others, especially fine-pitch surface mount components and certain new connectors, are dimensioned using SI units. This procedure is expected to continue for the foreseeable future.

The ETF provides dimensioning data in the "natural" units for each component type, including PWBs. Standard conversion factors may be applied as needed and appropriate.

Chapter 2: Principles for Design Optimization

This chapter is an overview of the major aspects of the module design process. It describes the factors that most impact the cost, quality, and time-to-market of a module.

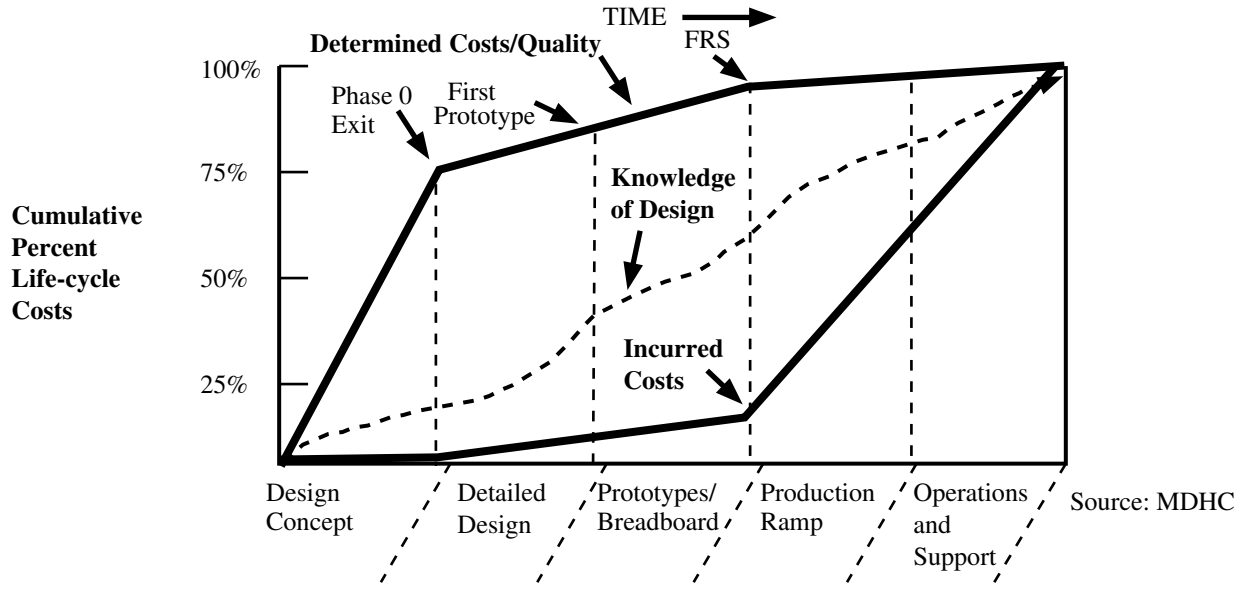
This chapter contains information for a concurrent engineering team to evaluate high level decisions within and across the module disciplines. The chapter focuses at present on the following module disciplines: Component, Connector, and Printed-Wiring Board Technology selection and Module Assembly and Test process design.

The introductory section presents the high level interactions between the module disciplines, describes the impact of using new technology, and presents some general guidelines. Each subsequent section contains guidelines and references to the detailed information contained in the corresponding ETF chapter.

2.1 Impact of Design Choices

The early stages of design have a significant impact on the life of the product. Although there is usually little incurred cost in the concept development phase, the design choices made at this point have a considerable impact on the total product cost. Figure 2-1 shows the typical relationship between determined and incurred product costs.

Figure 2-1: Determined and Incurred Product Costs

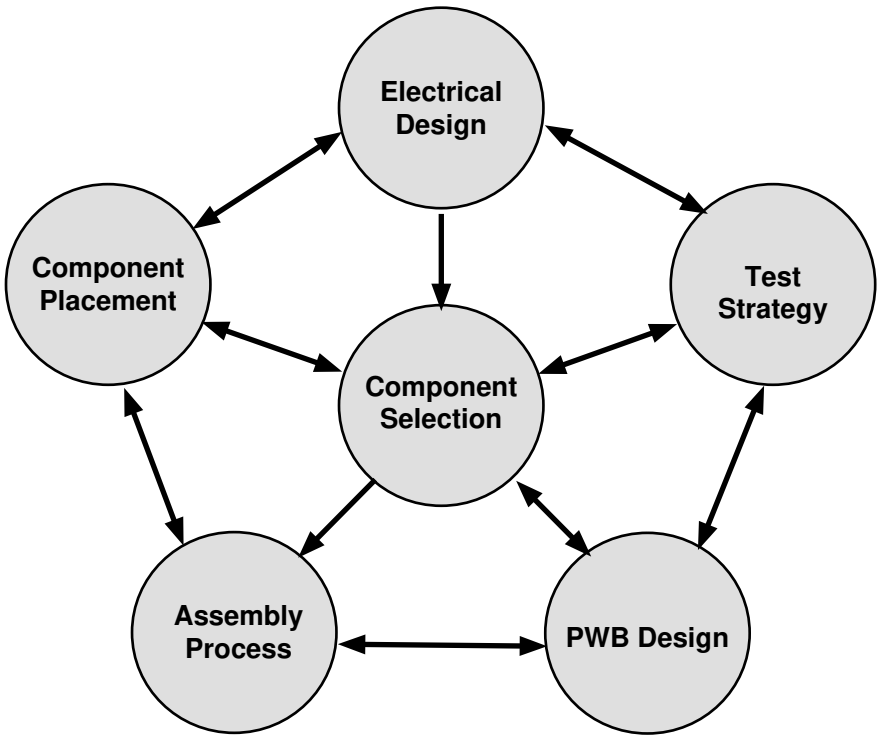


In the initial stages of product design, when concept and architecture decisions are the predominant activity, there are usually a few key people involved and spending levels are relatively low. As the product becomes better defined, there is more activity and spending. In the typical life cycle of a product, a great deal of time and money is spent testing and reacting to decisions that are made in the early phases. Risk can be managed by increasing the knowledge of the design through analysis and experimentation early in the design process so that the product will have a better chance of success. Working

with representatives from key organizations on a concurrent engineering team will also aid in the assessment of the downstream impact of design decisions.

The process of defining the physical architecture of a product involves optimizing a number of factors that are interrelated. Module design choices drive process design choices. Conversely, process constraints often provide design constraints. Each product has performance, cost, quality and time-to-market goals. Design decisions should be based upon information from all aspects of design and manufacturing and an understanding of how those decisions affect the product goals. Figure 2-2 illustrates the complex interactions between the major design and manufacturing disciplines.

Figure 2-2: Interrelationships between Design Choices and Manufacturing Process



Component selection, both mechanical and functional, is the key design decision which has far reaching implications for the product. It affects not only PWB design , but also assembly and test process design, often having unforeseen cost, quality and time-to-market effects on the product. Component selection becomes even more critical when the use of a new technology is involved. The cause-effect relationships between design decisions and manufacturing can be found in Figure 2-3.

This chart represents choices made within the Electronics Packaging Working Group (EPWG) MP4 Technology Platform. If design choices are made outside of this, they may have a significantly different impact.

Figure 2-3: Manufacturing Impact of Design Choices

Manufacturing Impact / Design Choices	PWB	Assembly Process			Test Process		
		Process Flow	Process Cost and Quality	Product Reliability	ATE/ In-Circuit Test	Functional Test	Stress Screening
Component Selection							
Pitch	●	●	●				●
Package Style	●	●	●	●			
Power	●			●		●	●
Size	●	●	●	●			
Total I/O	●	●	●		●	●	
Operating Frequency	●				●	●	●
Edge Rate					●	●	●
Tri-stateability					●		
Connector Selection							
Pitch	●		●		●	●	
Size		●	●		●		
Total I/O			●	●	●	●	
Signal:Reference Ratio					●		
Board Attachment	●	●	●			●	●
PWB							
Size	●	●	●	●			
Surface Finish		●					
Materials	●	●					
Routing/Dispersion Grid	●		●		●		
Electrical Characteristics							
Device Isolation					●		
Operating Frequency				●	●		
Diagnostic Implementation						●	●
Controlled Impedance	●						
Component Placement							
Side of Module	●	●			●	●	
Grouping	●	●			●	●	
Clearances	●	●	●	●	●	●	
Orientation		●	●				

2.1.1 Use Of New Technology

One design choice that has a major impact on the cost, quality and timeliness of new product introduction is the use of new technologies. When a design choice requires the use of a new or unproven technology or process, time and money will be required to develop the necessary components and processes. A component or technology which is new to Digital but proven in the industry is less of a risk than a component or technology that is new to Digital as well as new to the industry.

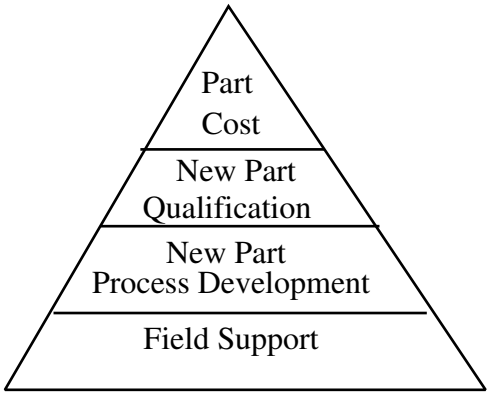
New packages must be qualified to ensure adequate thermal, mechanical and electrical properties. Furthermore, most new packages or parts require some manufacturing process development. This development can range from the fixture design to a large scale development project involving associated capital and engineering costs.

Cost Impact:

New technology choices affect module cost. On a typical module, the materials cost represents 90 to 95% of the standard module cost. Module assembly and test value-added costs range from 5 to 10% of the standard module cost. However, the introduction of new technologies in the form of new package styles, or industry unique components which spawn the need for new manufacturing processes, can significantly increase the value-added cost as a percentage of total module cost and can significantly impact process quality and time-to-market.

Often the cost associated with the purchased part is only the beginning. Figure 2-4 illustrates this analogy. Engineering start-up costs are often significant and should be considered. Every time a new assembly step is developed, a new repair step needs to be developed. Moreover, the cost to maintain the new technology in the field often outweighs the manufacturing cost.

Figure 2-4: Amplification of Costs for a New Component



Quality Impact:

New technology choices often have associated high defect levels in the manufacturing process. These yield problems manifest themselves due to a variety of reasons including vendor quality and process immaturity. Quality problems not only increase repair costs during the manufacturing process but also affect cycle times and inventories. As defect levels increase, more testing, diagnosis, and repair is required, thereby increasing the time required to produce the product. Use of immature technology can be especially troublesome in the prototype phase where time to produce the product may directly affect time-to-market.

Time-to-Market Impact:

As mentioned above, new process development and component qualification take time. In today's competitive environment, reducing time-to-market is increasingly important. Time-to-market can be minimized by taking advantage of mature package and process technologies wherever possible. When selecting a new technology, risk should be managed to understand the impact of this choice as early and completely as possible.

Early analysis of cost, quality and time-to-market impact will help to manage the risk associated with unproven technologies or processes. Early modeling and experimentation can be done to understand and identify any unforeseen effects that might arise in the manufacturing process. Furthermore, robust design techniques can be helpful in reducing component costs and increasing the associated quality by reducing the product sensitivity to variations in components and variations in the manufacturing process.

2.1.2 General Guidelines

The following guidelines describe some general principles of design for manufacturability and testability.

1. **Involve manufacturing** as early as possible in the design process in order to optimize the design with respect to cost, quality and time-to-market.
2. Use the **simplest** solutions that meet cost and performance objectives.
3. Use new technology **only** when necessary.
4. **Emphasize standardization**, particularly with parts and materials
5. **Minimize the number and types of parts in the design**. Each part number adds cost to the process in the form of setup, opportunity for error, capital, inventory and other overhead.
6. **Avoid expense and capital cost**. Ensure that capital cost with respect to volume is included in product cost estimates. Ongoing expenses such as fixture and machine maintenance should also be considered.
7. **Ensure footprint pad and part dimensions are compatible**. Errors are easily overlooked but can cause major problems when part and pad dimensions do not match.

8. **Allow for variation of parts** within their specification limits, both electrical and mechanical.
9. Select **testable components** and design for testability.

2.2 Component Selection

Component selection is the **major** driver of module manufacturability and testability. The choices made at this phase of the module design have a significant impact on new product start-up costs, assembly process cost and quality, and test process cost and effectiveness.

Additional information in component selection can be found in Chapter 3, LSI Chip Packaging, and in Chapter 4, Active and Passive Components.

2.2.1 Component Selection Guidelines

To ensure that process cost, quality and time-to-market (time to steady-state manufacturing) are optimized, follow the guidelines listed below.

1. **Use parts on the ETF Preferred Parts List**[1]. Parts found on the ETF Preferred Parts List have proven manufacturability, and other preferred attributes, such as lead time, cost, and quality.

Part Selection Criteria	Order of Preference
Common parts across product families Commodity Parts Digital Specials	↓

2. **Design to minimize the number of part numbers.** The quantity of part numbers affects module complexity, the size of the assembly line, set-up times, material acquisition, and stockroom costs. Not only are direct costs reduced, but also opportunities for defects are reduced resulting in lower repair and test costs. **An example** of how to minimize the quantity of part numbers is to reduce the number of different resistor values used on a module and standardize on 1% tolerances.
3. **Use common parts across product families.** This reduces inventory control and maintenance costs in the manufacturing plants.
4. **Design to minimize the number of components requiring hand insertion**, especially those requiring both hand insertion and hand soldering. Examples of these are:
   - Components that overhang the board
   - Components that do not meet height restrictions
   - Components that are not compatible with assembly processes

[1] The ETF Preferred Parts List will be available as part of Chapters 3 and 4.

5. **Choose components that enable testability**. Attributes that enable testability are Built-In Self Test (BIST), JTAG, Tri-stateability, and so on.
6. **Select components to achieve the simplest assembly process flow** in order to minimize the number of process steps and the number of thermal cycles that the module will undergo. Additional process steps add opportunities for defects. Additional thermal cycles may affect reliability. See Figure 2-7.
7. Minimize the number of **programmable components.**
8. **Consider Material Acquisition issues** such as number of vendors and lead times for parts.

The following **additional** guidelines should be applied when components are **not chosen** from the **preferred parts list.**

Part Selection Criteria	Order of Preference
Part on preferred parts list Existing Digital Qualified part/package New part to Digital but industry standard * New part to Digital from qualified vendor * New part to Digital with new manufacturing process requirements *	

* See Component Engineering for Part Number assignment

1. **Design to minimize the number of new part numbers.** Each new part number incurs component qualification costs. In addition, the average component maintenance cost is $6000 per year.
2. **Avoid new and nonstandard package styles.** New package styles significantly impact module manufacturing new product start-up cost and time. A new package module process qualification can cost over $1,000,000.
3. **Ensure components not on the preferred parts lists are compatible with the module assembly process.** If components are not compatible with the module assembly process thermal, mechanical and chemical stresses, the component must be hand-placed and soldered, which incurs significant cost and adds a labor intensive process step.
4. **Ensure the component meets Digital general specifications.** Component placement codes and footprint patterns are generated from component general specifications. If the component does not meet the general specifications, there is a potential for mismatches between the component dimensions and the footprint dimensions, which results in a redesign of the PWB and the potential for scrap PWBs and components.

5. **Pay attention to vendor process capability to produce mechanically acceptable parts.** Often a new vendor can supply a few good parts for qualification; however, when the product volume increases, the vendors volume process cannot consistently produce parts compatible with Digital assembly processes. This leads to ongoing quality problems over the life of the product and can affect the ability to ship product. Be prepared to put an ongoing quality audit program in place with the vendor.

2.2.2 Component Selection Design Trade-offs

Silicon integration is one method by which the number of components on a module can be decreased, potentially improving performance by reducing the number of pins. The use of a custom-designed integrated circuit to replace multiple standard components is a trade-off which affects many aspects of module design and manufacturing. A number of factors that affect the final cost of the module have to be considered when evaluating this design option.

Material Cost

1. Cost of the Advanced Silicon Integrated Circuit (ASIC) package versus the non-ASIC packages
2. Component qualification costs and materials acquisition costs
3. Changes in the cost of the PWB

Assembly Cost

1. Direct labor (is ASIC more complex, requires special processing?)
2. Indirect labor (special process development required?)
3. Cost of Scrap (new component quality issues
4. Repair and test cost (new component quality and reliability issues)

Time-to-Market Impact

1. Incremental chip development time
2. New component quality problems delay new product start-up

On-board module power can be implemented by using a number of commodity single-output power supplies in parallel or one multiple-output unit. Low power requirements can be obtained by using individual discrete components or units packaged and sold as single components. Trade-offs in development cost, individual output control, supplier availability, reliability and manufacturing compatibility must be considered.

2.3 Connector Technology Selection

2.3.1 Connector Selection Guidelines

The following is a generalized approach to connector selection.

1. **Define application**. A prerequisite to identifying a specific connector component is the definition of the application that is: Board-to-Board, Cable-to-Board, Cable, Socket, Power, and so on. Further definition may be added if it is a standardized application such as a Standard Bus (XMI, Futurebus), Standardized Interface (SCSI) or Standard Application (SIMM Socket).
2. **Define design requirements**. A second prerequisite is a detailed definition of the application specific design requirements. These will include a number of the following: pin count, footprint/density, orientation/geometry, PWB attributes, electrical performance, cost target, power requirements, keying, latching, product life, repairability requirements and durability.
3. **Define process requirements**. A third prerequisite is definition of process requirements. In the case of board mount connectors or sockets, the use of solder tail (Through-Hole), press pin or SMT options must be considered with respect to the overall PWB process predicated by other components. Similarity, in the case of cable applications, options must be considered such as solder, crimp, insulation displacement, and so on.
4. **Use Preferred Parts as first choice**. Components from the ETF Preferred Parts List (PPL)[1] should be used when possible. Components in the PPL generally are active parts currently used in Digital, best "type" in terms of cost and/or performance, qualified, supplied by a vendor on the Approved Vendor List (AVL), and supported by an established assembly process in one or more Digital facilities.
5. **Consider Cost.** The principal factors influencing the cost of connectors are volume, electrical performance (signal-to-ground ratio), size and metallurgy.
6. **Reduce options.** Two or more components may meet a number of the defined requirements. Selection of the "best option" will require further investigation including comparative analysis, testing, prototyping or modeling. Some of the more critical trade-offs are identified in **Section 2.3.2**.
7. **Restrict Introduction Of New Connectors.** In the event that a component from the PPL cannot be used, the introduction of a new component should be restricted to the following:
   a. Variants of existing parts in the PPL
   b. The need to meet a widely used industry standard
   c. Cost reduction

[1] The ETF Preferred Parts List for Connectors will be available as part of Chapter 5.

d. Performance enhancement

e. No Digital specials

8. **Consult Resident Expertise.** If the introduction of a new connector is indicated, you are advised to consult one of several individuals in Digital with connector experience. These personnel are resident in the Canadian Technology Center or the Component Engineering group. Involvement of a connector supplier should only occur when all other alternatives do not provide a suitable solution.

2.3.2 Connector Selection Design Trade-offs

The following is a list of the more critical trade-offs in the selection of connector components. **Chapter 5** of the Techfile will be useful for guidance in making these trade-offs..

1. **Electrical Performance versus Cost** will be influenced by the type (physical construction) of the connector as well as the choice of signal-to-ground ratio.
2. **Board Attachment Process** can be solder tail (through-hole), press pin or SMT. Trade-offs must consider the overall manufacturing process for the board, type of components on the board, and physical attributes of the PWB, such as tolerance requirements and board thickness.
3. **Contact Density** is defined in terms of lines per inch or lines per square inch and is influenced by many considerations including board layout, signal line routing, number of layers, value of PWB real estate and packaging geometry. Trade-offs also include numbers of rows in 2 piece connections as well as contact pitch 0.100 inch versus 2mm.
4. **Dedicated Power versus Use Of Signal Pins** becomes a trade-off involving cost, total current requirement versus current carrying capacity of individual pins, and availability of power segments for some connector types.
5. **Edge Connectors versus Two Piece Connectors** trade-offs need to take many issues into consideration including gold plating cost on PWB, thickness and dimensional tolerances required on PWB, reliability of connection, and cost of connector.
6. **Cable Costs** need to be considered when choosing a connector. Connector trade-offs that enable simpler cabling solutions are often preferred.

2.4 PWB Technology Selection

PWB guidelines and trade-offs typically involve managing wiring density in some manner. The emphasis for a PWB designer is to balance attributes by trying to achieve the optimal mix between the following critical parameters: line width, spacing, layer count and hole size to achieve performance, cost and reliability goals.

2.4.1 PWB Technology Selection Guidelines

The following are the major guidelines for printed-wiring board design and manufacture:

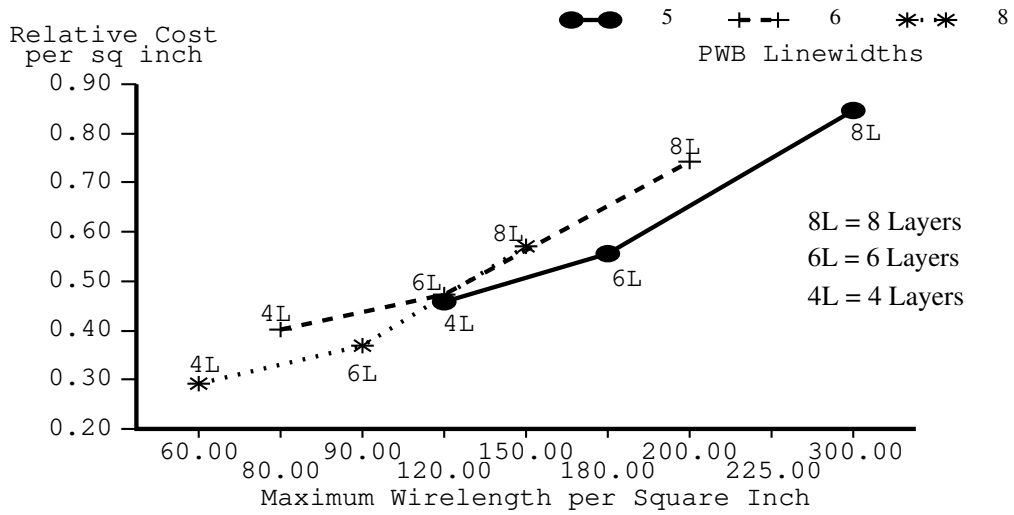
1. **Overall Size** - The most dominant factor in PWB cost is size; extra efforts should be made to minimize size whenever possible.
   - Try to utilize square or rectangular shapes.
   - utilize PWB and module manufacturing experts, eliminate or minimize test coupons or tooling strips.
   - Small form factor, inexpensive modules may allow the opportunity to eliminate in-circuit test and repair. This may allow a reduction in component to component spacing. See **Chapter 7, Module Layout Design Requirements.**
   - **Line width and Spacing** - The critical factors in line width selection are
   - Line widths down to 0.005 inch deliver the best interconnect value provided relatively full channel utilization across a signal layer compared to coarser lines and spaces. See **Chapter 6, Printed-Wiring Boards.**
   - A line width to space ratio of 1 to 1.5 or greater is preferred
2. **Layer Count** - Traditionally, PWB signal layers are added as orthogonal pairs for signal layers and power/ground pairs for reference layers. Consider the following when adding layers to a design:
   - Not every signal layer pair needs to have a reference layer pair added
   - Analyze using finer line widths and reduced via/pad sizes to reduce via/pad sizes to reduce layer count
   - Outerlayer signals should be used whenever possible to reduce layer count
3. **Via/Pad Selection** - Finer vias add more cost, but far more value when coupled with the appropriate line widths and spacings. The following should be considered in via selection:
   - PWB thickness to hole size ratio of 5:1 are routine.
   - Finished hole size selections down to 0.015 inch are not a technological or major cost impact.
   - Assembly and test process capability**.**
4. **Cost Adders** - The following cost adders should be carefully considered before being used.
   - Polyimide or other advanced material.
   - Controlled impedance to ± 10% tolerance
   - Gold plating
   - Tight tolerancing for line widths, dielectrics, hole true position**.**

5. **Noncost Adders -** The following do not add or add minimal cost to a **raw PWB**:
   - SMT pitches down to 0.5 mm
   - Single or double-sided component placement
   - Partial or full utilization of signal channels on a PWB layer
   - PWB thicknesses between 0.030 inch and 0.062 inch

2.4.2 PWB Technology Selection Trade-offs

- **Single versus double-sided** - The placement of SMT passive parts or memory parts on side 2 can reduce overall PWB size and increase component density with minimal compromise in wireability. Benefits of size reduction should be weighed against the cost and quality impact of extra assembly steps.
- **Line width verses layer count -** Various combinations of layer count and line width should be considered that may provide the optimal value for the component types selected. See Figure 2-5 to estimate cost for increasing layer count or decreasing line width.

Figure 2-5: Line width versus Layer Count Cost Data



- **Signal integrity versus wireability** - Signal integrity constraints for cross-talk may require large space to line width ratios resulting in a decrease in PWB wireability.
- **Grid selection -** Grid selection is crucial. It determines not only whether vias and holes are placed on a 0.050 or 0.100 inch grid, but it also requires line and space selection be balanced within the grid selected.

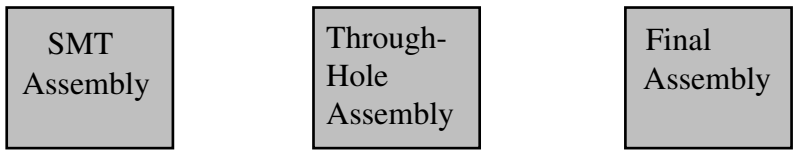
2.5 Assembly Process

This section describes the design choices that most affect the Module Assembly process. It contains descriptions of module process design and some high level guidelines and trade-offs of which the design team should be aware of to optimize the cost and quality of the module. Detailed information regarding cost and quality associated with a particular decision is found in **Chapter 7**, **Module Layout Design Requirements**.

2.5.1 Background

Typical Assembly Process Elements are shown in Figure 2-6. The types and locations of components determine which steps may be used, repeated or eliminated.

Figure 2-6: Typical Module Assembly Process Elements



SMT Assembly consists of the following major process elements: solder deposition, component onsertion, reflow, cleaning and visual/mechanical inspection.

Through-hole Assembly consists of the following major process elements: component preparation, component insertion, wave solder, cleaning and visual/mechanical inspection.

Final Assembly consists of component preparation, hand insertion/onsertion, hand soldering,and visual/mechanical inspection.

2.5.2 Module Assembly Process Design

The mixture of package styles that must be assembled on the module and their location determines the module assembly process complexity. Attributes that increase the module complexity are;

- Use of many different types of packages
- Nonoptimized placement of components (See **Chapter 7,** Module Layout Design Requirements)
- Number of thermal cycles
- Number of process steps

Figure 2-7 details how the choice and placement of components affects the assembly process design and shows the relationship to the number of thermal cycles and process steps. In general, the greater the complexity of the module and assembly process, the higher the opportunities for defects and reliability problems.

Figure 2-7: Module Assembly Process Design

Design Paradigm							
Type	Component Placement		Grouped for Shielding	Process Flow [1]	Thermal Cycles	Process Steps	Order of Preference
	Side 1	Side 2					
100% SMT	Actives and Passives [2]	None		A	1	5	Most Preferred
100% TH	Actives and Passives	None		B	1	5	
100% SMT	Actives and Passives	Passives		A + A	2	10	
	Actives and Passives	Actives Passives		A + A	2	10	
MIXED	SMT Actives and Passives TH	None		A + B	2	10	
	SMT Actives and Passives TH	SMT Passives		A + C + B	2	13	
	SMT Actives and Passives TH	SMT Passives SMT Actives	YES	A + A + B	3	15	
	SMT Actives and Passives TH	SMT Passives SMT Actives	NO	A + A + D	3	16	
	SMT Actives and Passives TH	SMT Passives SMT Actives TH	YES	A + A + B + D	4	21	
	SMT Actives and Passives TH	SMT Passives SMT Actives TH	NO	A + A + D + D	4	22	Least Preferred

1 A = SMT Assembly/Reflow, B= TH Assembly/Wave, C = Adhesive Deposition, D = Selective Solder
See **Section 7.6.1** for detailed explanation of A,B,C, and D of Process Flow Column.
2 Passives = 2 leaded devices, Actives = >2 leaded devices

Notes:

On double-sided mixed-mount modules, the grouping of the through-hole components is important such that the side 2 SMT components can be shielded during the wave solder process. See Chapter 7, **Rule 4-5.** The ability to shield these components will determine whether the **preferred** solder wave process can be used or if the selective solder process needs to be used for through-hole assembly.

Hand assembled components add a level of complexity to each of these paradigms. **Chapter 7, Module Layout Design Requirements** describes these manual processes in terms of number of steps and cost.

Repair and PWB fabrication also expose the module to additional thermal cycles and should be considered during reliability calculations.

2.5.3 Module Assembly Considerations

1. Select process and design features that **minimize the number of thermal cycles** during assembly. For example, single-sided surface mount is preferred over double-sided. Note: the intrusive reflow process is not yet available.
2. Select process and design features that **minimize the number of process steps**.
3. Push for **part homogeneity**. On a mixed-mount module, limit through-hole parts to those that do not have a proven SMT alternative such as Pin Grid Arrays (PGAs), connectors and so on.
4. **Verify component and footprint dimensions** match. This will avoid significant cost and time delays during the prototype and production phase of product introduction.
5. The **integrity of the manufacturing data and documentation** is critical to timely new product start-up and ramp to volume manufacturing . See Chapter 9, Product Data, for more information.
6. On a mixed technology module, the **preferred process to assemble through-hole components is the solder wave.** Selection and placement of components, as well as clearances will determine if the solder wave process can be used. See Figure 2-9 and Chapter 7, **Rule 4-5,** for guidelines for a wave solderable module. The alternative process is the selective solder process which is not a high volume process and is not as mature as the solder wave process.
7. The module should be designed such that its **thermal profile in the reflow process is uniform.** This is done by making the layout of the PWB and the placement of the components as uniform as possible. However, this must be traded-off with requirements of the other process elements. To facilitate the soldering processes, SMT and TH components should be grouped together in a mixed mount module for shielding. Minimizing the gross distances between fine pitch components tends to minimize defects in their placement and reflow. All these things must be considered and optimized in the layout of the circuit.
8. **Minimize opportunities for defects.** Minimizing the number of parts in the design and minimizing the number of process steps in manufacturing results in a reduction in opportunities for defects. By understanding the defect levels associated with the various processes, the overall defect level of the product may be reduced during the design phase.

2.6 Test Process

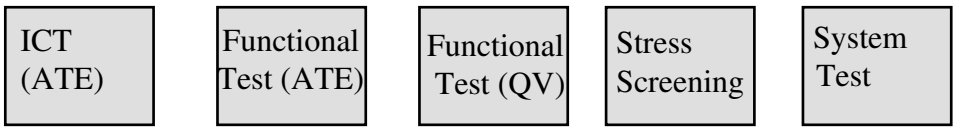
This section describes what design choices most affect the module test process. It contains descriptions of a few high level guidelines and trade-offs of which the design team should be aware and work early on to optimize the cost and quality of the module.

Refer to Chapter 7, Module Layout Design Requirements, Chapter 10, Module Cost and Quality Estimation (in process), and Chapter 14, Design and Product Verification (in process), for additional information on requirements, cost, quality and strategy test.

2.6.1 Background

Typical Test Process Elements are shown in Figure 2-8. The decision to use one or more of these test steps is product specific and should take into consideration the level of testability incorporated into the design, the projected fault profile of the module and the expected total defects per unit (TDU) levels.

Figure 2-8: Typical Test Process Elements



In-Circuit Test Using Automatic Test Equipment (ATE)

In-circuit test using ATE is used to identify manufacturing-induced faults by isolating and individually testing devices using a bed of nails fixture. This set of faults typically includes shorts, wrong-valued analog parts and opens that manifest themselves as stuck-at-one or stuck-at-zero failures. Depending on the test equipment, the patterns are executed at a frequency of 10 MHz or less.

Functional Test Using ATE

Functional test using ATE is used to identify manufacturing induced faults by stimulating the module from the edge and testing the module as a whole. This set of faults typically includes shorts, wrong-valued analog parts, and opens that manifest themselves as stuck-at-one or stuck-at-zero failures. Depending on the test equipment, the patterns are executed at a frequency of 10 MHz or less.

Functional Test Using a Functional Test Station

The intent of a functional test is to identify module level functional faults. This includes manufacturing induced faults that escape from previous test steps, as well as timing-related failures and faults internal to components on the module. The station operates at the frequency the module was designed for and may have the capability to margin temperature, voltage, and frequency.

Stress Screening

The intent of stress screening is to precipitate infant mortality failures. A stress screening chamber is used to thermal cycle the modules under test. Depending on the implementation, the module could be executing tests during the cycling and may or may not be powered up during different portions of the temperature cycling.

System Test

The intent of system test is to identify modules that do not function within the system environment for any reason.

2.6.2 Module Test Process Design

The factor that most affects the test process design is the level of defects in the module. Typical TDU levels of 3 to 60 prevail in most plants for the majority of modules. The manufacturing test cost to find and fix defects is about $6 per defect. As TDU levels are decreased below 1, test steps can be eliminated and test costs can be significantly reduced.

Figure 2-9: Module Test Process Design Preferred Attributes

Preference	In-Circuit Test	Functional Test	Stress Test
Most Preferred ↓ Least Preferred	One test point per node Standard Pad Sizes(.040-.035 inch) All devices tri-stateable Implementation of JTAG ↓ Double-sided actives Limited physical node access Use of Non-tri-stateable devices Small pad sizes (.035-.032 inch)	Product level BIST (Power only test bed) ↓ Downloaded test using off the shelf capital ↓ Downloaded test using custom configurable tester/test bed ↓ Downloaded test using designed module specific tester/test bed	Product level BIST w/remote initiation and failure sense capability, stress performed in generic plant thermal chamber ↓ Downloaded test using capital that enables remote test execution and reporting, stress performed in generic plant thermal chamber ↓ Downloaded test using custom capital that requires custom stress/thermal capability

2.6.3 Module Test Consideration

A. ATE Options: Functional, In-circuit or None

The decision on whether or not to include an ATE step in the test process should be based on the predicted fault profile. If the module technology allows for the use of well-understood and controllable assembly processes, manufacturing induced faults might be low. It could be cost effective in this case to eliminate ATE from the test process and allow faults to pass to the functional test step.

In most cases, the decision between using the ATE to perform an in-circuit or functional test is made based on technology and module layout. In-circuit testing imposes several requirements on both the design and the layout (See **Chapter 7, Module Layout Design Requirements**), while functional ATE applications require large simulation efforts and are more complex..

B. In-Circuit Test Trade-Offs/Considerations

1. Accessibility

(a) Test Pad Size versus Signal Integrity Concerns
Product team must balance the need for 0.035 inch minimum test pads with the signal integrity needs of the product. Smaller test pads can result in less reliable tests or the elimination of ICT as a feasible test step.

(b) Side 2 Access and Clearances versus Layout Density
ICT places several requirements on the layout in terms of accessibility and side 2 placement density . See Chapter 7, Rules 5-1 and 5-3. These requirements must be balanced with the speed requirements and functionality of the product and trade-offs made when necessary.

2. Test Probe Placement

ICT requires electrical access to each network, including unused outputs, on side 2 of the module. To minimize the capacitive effects of the test fixture, it is preferable to place the test probe on, or as close as possible, to the network's driver. However, trade-offs must be made if test probe density exceeds a critical number and a mechanical overclamp is not desired or if the layout does not permit such placement.

3. Device Isolation

(a) In order to execute a reliable in-circuit test, each device-under-test must be isolated from all other components on the model. This is done by tri-stating devices where possible, or by preconditioning signals away from ground to avoid back-driving. Trade-offs must be made between test complexity and device selection when comparable, tri-stateable versions of devices are available.

(b) It is also necessary to break feedback loops on the module. Trade-offs must be made between test complexity and additional logic that can be used to break feedback loops but could affect performance.

4. **Operating Frequency, Edge Rates, Signal Integrity**

   In-circuit ATE applications execute at the operating frequency of the test equipment which is typically slower than that of the module. Without jeopardizing product functionality, select components which will tolerate the lower frequencies and slower edge rates of the test equipment whenever possible.

5. **Module-Only Self-Test**

   Self-test can be executed using ATE if the code is written such that responses are not required from sources off the module. Trade-offs must be made between the effort required to structure the code in this manner and the possibility of deleting the functional test bed from the module screen process.

C. Functional Test Trade-Offs/Considerations

The test equipment for this test step can vary greatly depending upon the module design and the diagnostic software. The simplicity of using a power-only test bed must be traded off against the effort to implement module level built-in self test. From module manufacturing's perspective, a power-only test bed is most preferable while downloading code from a custom-designed test bed is least preferred.

Diagnostic isolation is a major concern at the functional test step. Manufacturing benefits from designing the layout to allow for the use of component vacuum clips, adding LEDs to indicate failures, and providing EEPROMs to log failure data on the module. These benefits must be traded off against the possible impacts to module functionality.

D. Stress Screening Trade-Offs/Considerations

The preferred method of stress screening in volume manufacturing is to execute a module level, built-in self-test while being able to easily monitor the status bit(s) in a generic thermal chamber. The ease of implementing this type of test must be traded off against the design constraints imposed by requiring dedicated connector pins for test. In addition, part selection can be influenced in an effort to keep the thermal envelope as wide as possible.

Least preferable at this step is to have the design require custom equipment with thermal cycling capability built in. This occurs when the design does not allow for the necessary test hooks mentioned above.

Chapter 3: IC Packaging

This chapter covers the packages which are recommended for use within the guidelines of the Corporate Packaging and Interconnect Strategy. Complex through-hole and surface mount packages are covered, as well as older (such as dual in-line packages) and less complex surface mount (memory packages, small outline packages) styles.

The information contained in this chapter is intended to be relevant to the end user of integrated circuit (IC) components. The material does not cover the details of design and performance modelling, areas which tend to be specific to the supplier of ICs. However, pointers are provided to documents which cover those topics in detail.

3.1 Primary Package Technologies

Three construction technologies have been in prominance since the early days of IC devices. These technologies have and are still being applied to applications ranging from simple, low gate count components to the current, complex packages used for leading edge microprocessors. These base technologies are:

- Multilayer cofired ceramic (MLC): laminated and fired alumina ceramic with refractory interconnect traces and vias.
- Glass sealed ceramic with leadframe: Pressed alumina base and cap with sandwiched stamped or etched metal leadframe, sealed with glass.
- Molded plastic: metal leadframe encased in transfer molded plastic, usually thermosetting epoxy.

MLC technology now predominates in complex, performance driven packages. It is also the most expensive of the package technologies. Plastic dominates the lower performance realm and is the most inexpensive technology. Molded plastic comprises more than 93% of all IC packaging, based on current world wide IC production. Glass sealed ceramics have a niche position in applications where power levels exceed the capabilities of plastic.

A variety of package mechanical configurations have been produced based upon the above technologies. The two major groups are through-hole (for example, low pincount dual in-line packages and high pincount pin grid arrays) and surface mount packages. Two further classifications of surface mount packages include:

- J-Bend (lead wraps under package)
- Gull-wing (lead extends out from package)

The various pin configurations are depicted in Figure 3-1.

Representative packages based on the major technologies are depicted in Figures 3-2 through 3-5.

Figure 3-1: Package Pin Configurations

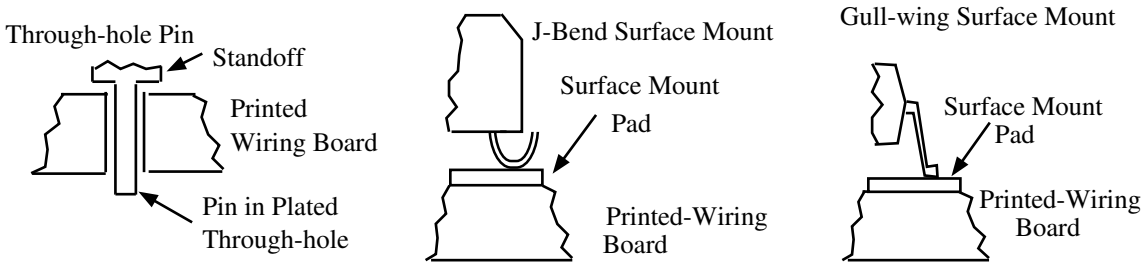
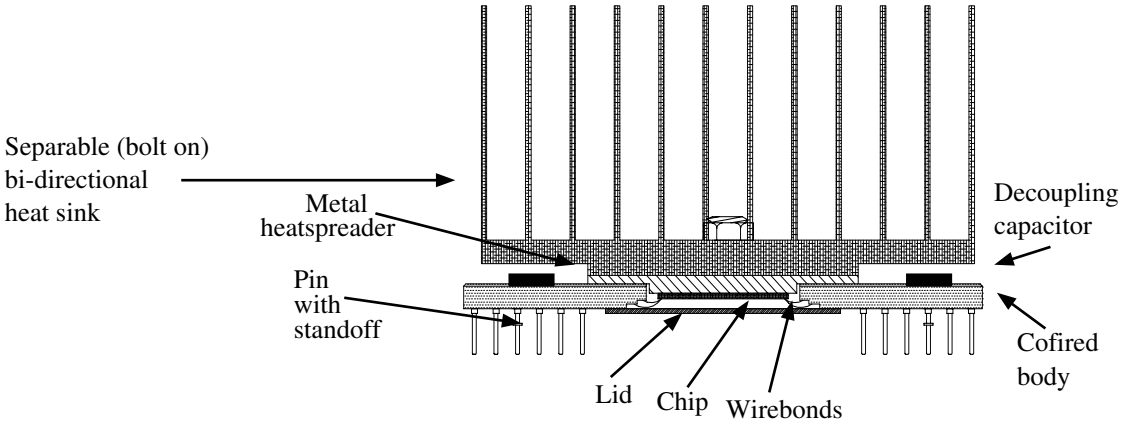
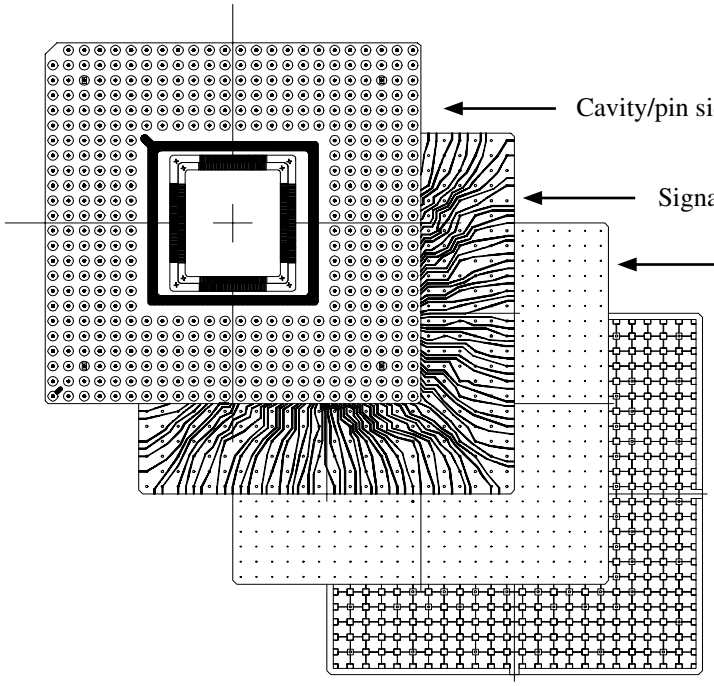


Figure 3-2: Performance Driven Package
EV4 Pin Grid Array - Multilayer Ceramic Design

This figure shows a highly evolved package which has been designed to the specific requirement of a high pincount, high power, high speed microprocessor. The package is hermetic: a solder sealed metal lid makes the chip cavity area gas tight.

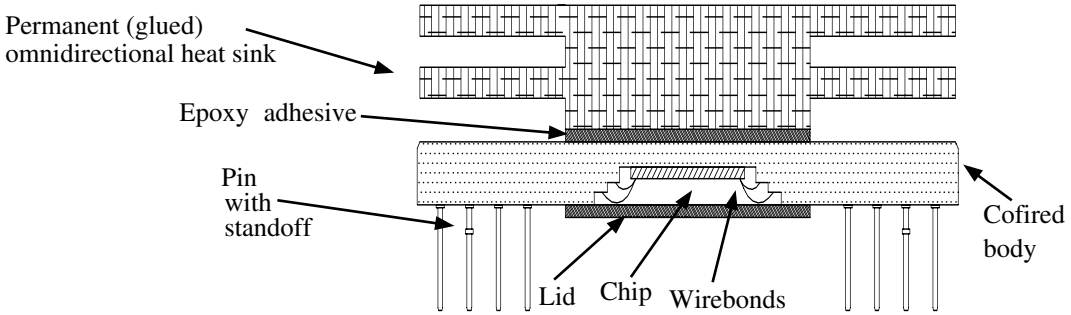


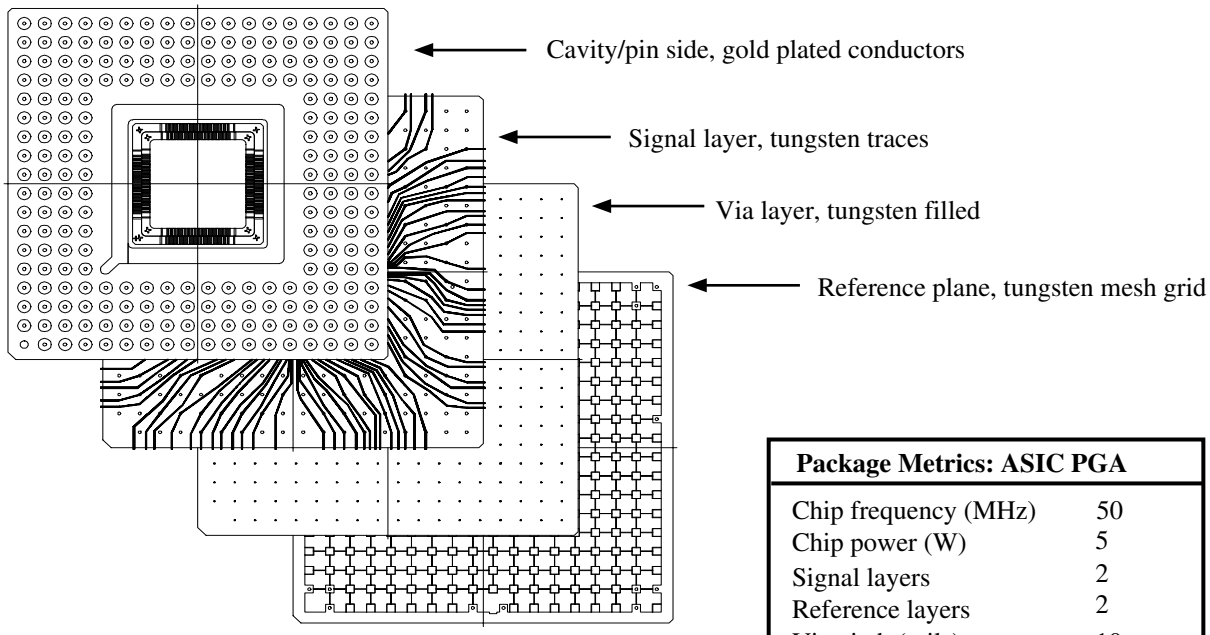

Cavity/pin side, gold plated conductors
Signal layer, tungsten traces
Via layer, tungsten filled
Reference plane, tungsten mesh grid

Package Metrics: EV4 PGA	
Chip frequency (MHz)	85
Chip power (W)	20
Chip pads/wires	428
Signal layers	2
Reference layers	6
Via pitch (mils)	9
Conductor line/space (mils)	5.5/5
Package body size (inches)	2.4
Package pins	431
Pin pitch (mils)	100
Package body	Alumina
External plating	Gold
Seal	Hermetic
Decoupling caps	14
Cost/package	$70.00
Cost/pin	$0.16

Figure 3-3: Cost/Performance Driven Package
ASIC Pin Grid Array - Multilayer Ceramic Design

This figure depicts a commodity version of Figure 3-2 suitable for moderate performance applications. Simpler construction and coarser features result in lower piece part costs.

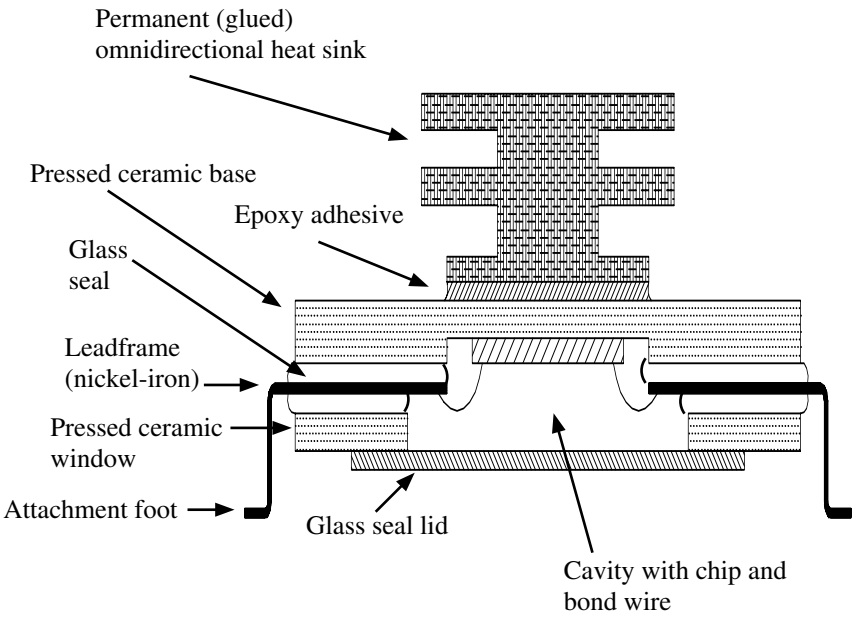


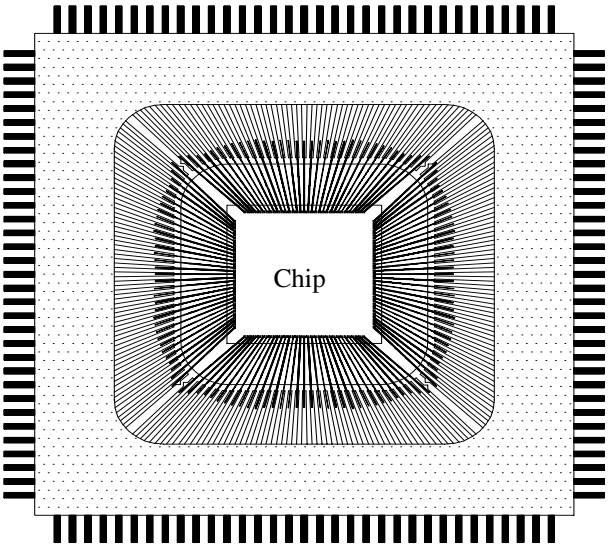

Cavity/pin side, gold plated conductors
Signal layer, tungsten traces
Via layer, tungsten filled
Reference plane, tungsten mesh grid

Package Metrics: ASIC PGA	
Chip frequency (MHz)	50
Chip power (W)	5
Signal layers	2
Reference layers	2
Via pitch (mils)	10
Conductor line/space (mils)	5.5/5
Package body size (inches)	1.8
Package pins	223
Pin pitch (mils)	100
Package body	Alumina
External plating	Gold
Seal	Hermetic
Decoupling caps	None
Cost/package	$26.00
Cost/pin	$0.12

Figure 3-4: Cost Driven Surface Mount Package Digital Cerquad, TANDU Device

This figure shows a hermetic surface mount package which is usable with lower performance devices which still may impose significant thermal requirements. This package style is, therefore, a bridge between the cost/performance PGA package and the electrically and thermally limited plastic package.



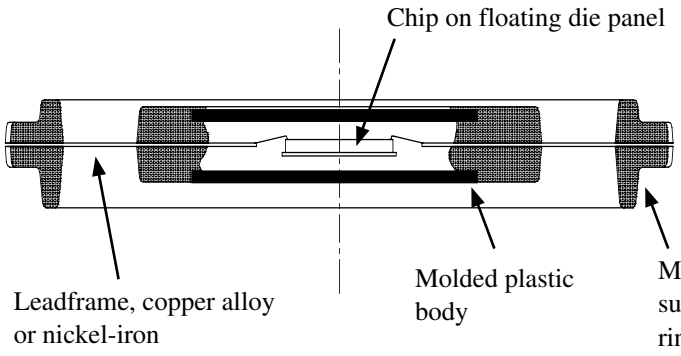


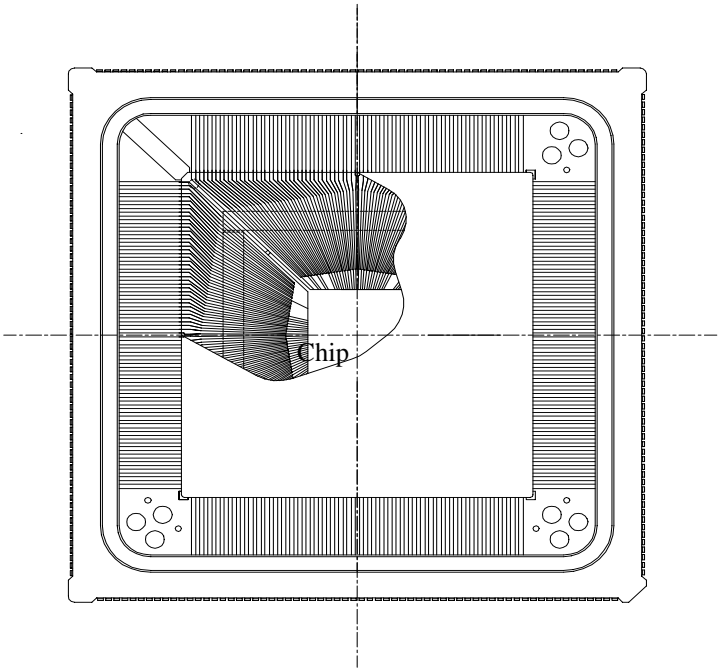
Cavity side view without lid

Package Metrics: TANDU Cerquad	
Chip frequency (MHz)	30
Chip power (W)	3
Package interconnect	1 level, leadframe
Package body size (inches)	0.9
Package pins	132
Pin pitch (mils)	25
Package body	Alumina
External plating	Tin
Seal	Hermetic
Cost/package	$11.00
Cost/pin	$0.08

Figure 3-5: Cost Driven Surface Mount Package Metric Plastic Quad Flat Pack (PQFP), TULIP Device

This figure shows an example of the dominant plastic surface mount metric standard format which has come into wide usage at high pincounts (100 through 240) and which is also displacing lower leadcount, English-dimensioned surface mount packages such as the plastic leaded chip carrier (PLCC). The package is shown prior to leadform (gull-wing) with an optional molded lead support ring in place. This ring protects the leads during post package assembly, handling and shipping. Lead forming may be done at any point from package assembly to just prior to module assembly.





Top view package and support ring

Package Metrics: TULIP PQFP	
Chip frequency (MHz)	30
Chip power (W)	1
Package interconnect	1 level, leadframe
Package body size (mm)	28
Package pins	208
Pin pitch (mm)	0.5
Package body	Epoxy
External plating	Tin/lead
Seal	Non hermetic
Cost/package	$2.50
Cost/pin	$0.01

3.2 IC Package Preferred Attributes

The following two tables provide detail on critical component external attributes from the perspective of modules assembly. Table 3-1 covers surface mount packages; Table 3-2 covers through-hole PGAs Some of these attributes are still being negotiated with the component suppliers. These are denoted by a shaded entry.

Table 3-1: Surface Mount

Package Type => Pitch => Unit unless specified =>	Cerquad 0.050inch 0.001 inch	Cerquad 0.025inch 0.001 inch	PQFP 0.65 mm mm	PQFP 0.5 mm mm	Notes
Lead Width	21.1 ± 2.5	13.1 ± 1.5	0.32 + 0.06 - 0.10	0.22 ± 0.05	1
Lead Thickness	8.6 ± 1.0	6.1 ± 1.0	.145 ± 0.055	0.145 ± 0.055	1
Skew	± 3.75	± 3.75	0.13	0.08	2
Tip-to-Tip Tolerance	± 5	± 5	0.20	0.20	
Coplanarity	4	4	± 0.10	0.08	
Foot Length	23 ± 5	23 ± 5	0.60 ± 0.15	0.60 + 0.15 - 0.10	
Standoff Height (High) (Low)	15	15	0.25 minimum 0.10 ± .05	0.25 minimum 0.15 ± 0.10	
Lead Material	Alloy 42	Alloy 42	Copper	Copper	
Lead Finish Metallurgy	Solder Dipped 350 ± 250µinch Matte Sn Plated 300-800µinch per side 63/37 Sn/Pb Plated 150µinch over 150µinch Ni				
Max Total Height w/ H/S	0.4		4.5		3
Max Total Weight w/ H/S	14g if pick-up surface <25mm; 20g if pick up surface > 25mm				4
Foot Radius	15 minimum	18 ± 4	0.14 ± 0.06	.165 ± .085	
Toe Angle	+1/-5 degree	+1/-5 degree	0/-7 degree	0/-7 degree	
Maximum Pkg Pin Count	84	164	232	240	5
Maximum Tip-to-Tip Size	1.89 x 1.89 inch		48 x 48		6
heat sink Location Tol	± 20		N/A		
P/U Surface Flatness	15mils/inch		0.1		7
Pick-Up Surface Parallelism	No HS: 6mils/inch W/HS: 8mils/inch		0.13		8

Notes for Table 3-1:

1. Dimensions include plating, that is, finished dimensions.
2. Skew is centerline deviation of a lead relative to its designed nomimal position.
    1. English pitch: According to 21-00019-GS, RFS applies.
    2. Metric pitch : According to JEDigital JC-11.11-92-159 (10/92), MMC applies.
3. Maximum total height is lead seating plane to top of pick-up surface and is (that is, heat sink or package) limited by Fuji IP-series machines to 0.4 inch.
4. Maximum total weight includes heat sink, if applicable, and is limited the free area available for the pickup nozzle. All fine-pitch placement machines utilize vacuum nozzle area. heat sink platter area, heat sink location tolerance, and part delivery to pick-up part tolerance all affect which nozzle can be reliably used. Thus a two stage specification is necessary:

    If pick-up surface < 25 mm diameter, then maximum payload = 15 gms.
    If pick-up surface >= 25 mm diameter, then maximum payload = 20 gms.
5. According to Electronic Packaging Working Group (EPWG) roadmap.
6. Maximum tip-to-tip limited by Siemens HS-series machines to 1.89 inch.
7. Pick-up surface flatness: either top of package or heat sink.
8. Parallelism defined by slope between packup surface and lead seating plane; note variation in specification depending on whether or not heat sink defines pick-up surface.
9. SOIC packages, though not included in the table, should follow equivalent pitch lead form tolerance specifications as Cerquads: skew, coplanarity, tip-to-tip.

Table 3-2: Through-Hole PGA

Package Type	PGA	IPGA
Pitch	0.100 x 0.100 inch	0.100 x 0.050 inch
Unit unless specified	0.001 inch	0.001 inch
Physical Size (max)	2.4 x 2.4 inch	2.2 x 2.2 inch
Max I/O	431	447
Max Rows of Pins	6	8
Material	Ceramic	Ceramic
Pin Diameter	18 ± 2	16 ± 2
Pin Length (nominal)	195	170
Pin Protrusion below PWB	38 ± 22	27 ± 3
Stand-off Height	50 ± 5	47 ± 5
Stand-off features	Center, rectangular geometry per GS specification in all four corners	
Length	50 ± 5	50 ± 5
Width	26 ± 5	26 ± 5
Thickness	8	8
Pin Mat'l and Finish	Kovar or Alloy 42 with Nickel overplate (minimum 100µinch)	
Pin Finish Metallurgy	Gold (Minimum 50µm or Solder 63/37 Sn/Pb (minimum 150 µinch) over nickel (minimum 100 µinch)	
Pin Positional tolerance (Pkg)	20	20
Pin Positional tolerance (Pin)	± 10	± 10
PGA Flatness	4 ± 1	4 ± 1

Note:

PGA pin lengths assume a 0.093 inch thick board. For other thicknesses, pin length is determined by (PWB thickness + standoff height + pin protrusion).

3.3 Preferred and Acceptable LSI Chip Packages

The following sections provide brief descriptions of each package type, by outline and technology, with cross references to the detailed Corporate general specifications. These specifications should be consulted when more information is desired. Each general specification is by package configuration and contains the following information:

- Other applicable documents (quality and reliability requirements, piece parts)
- Shipping requirements (packaging media)
- Lead finish specifications (materials, thicknesses, solderability standards)
- Body specifications (tolerances, workmanship)
- Leadform critical parameters (width/spacing, coplanarity, skew)
- Toleranced outline drawings

Each package is designated by mounting style (through-hole or surface mount) and suitability for cost effective, high yield assembly in stage 1 manufacturing.

IC packages are dimensioned in either English or metric units according to international standards.

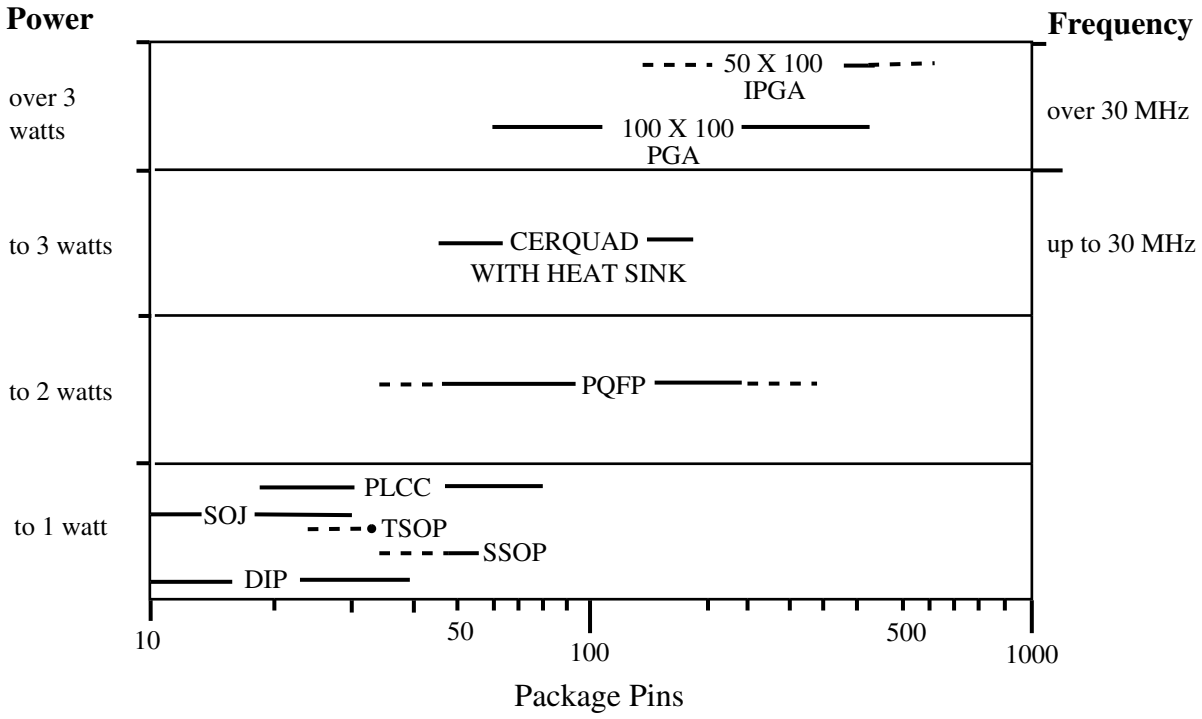
DIP, PGA, Cerquad, PLCC, SOJ, SOIC, and SSOP packages are English dimensioned. TSOP and most PQFP styles are metric dimensioned.

Pin pitches follow this practice even though it is not uncommon to confuse close equivalents (for example, 0.65mm and 25 mil).

3.3.1 Package Selection

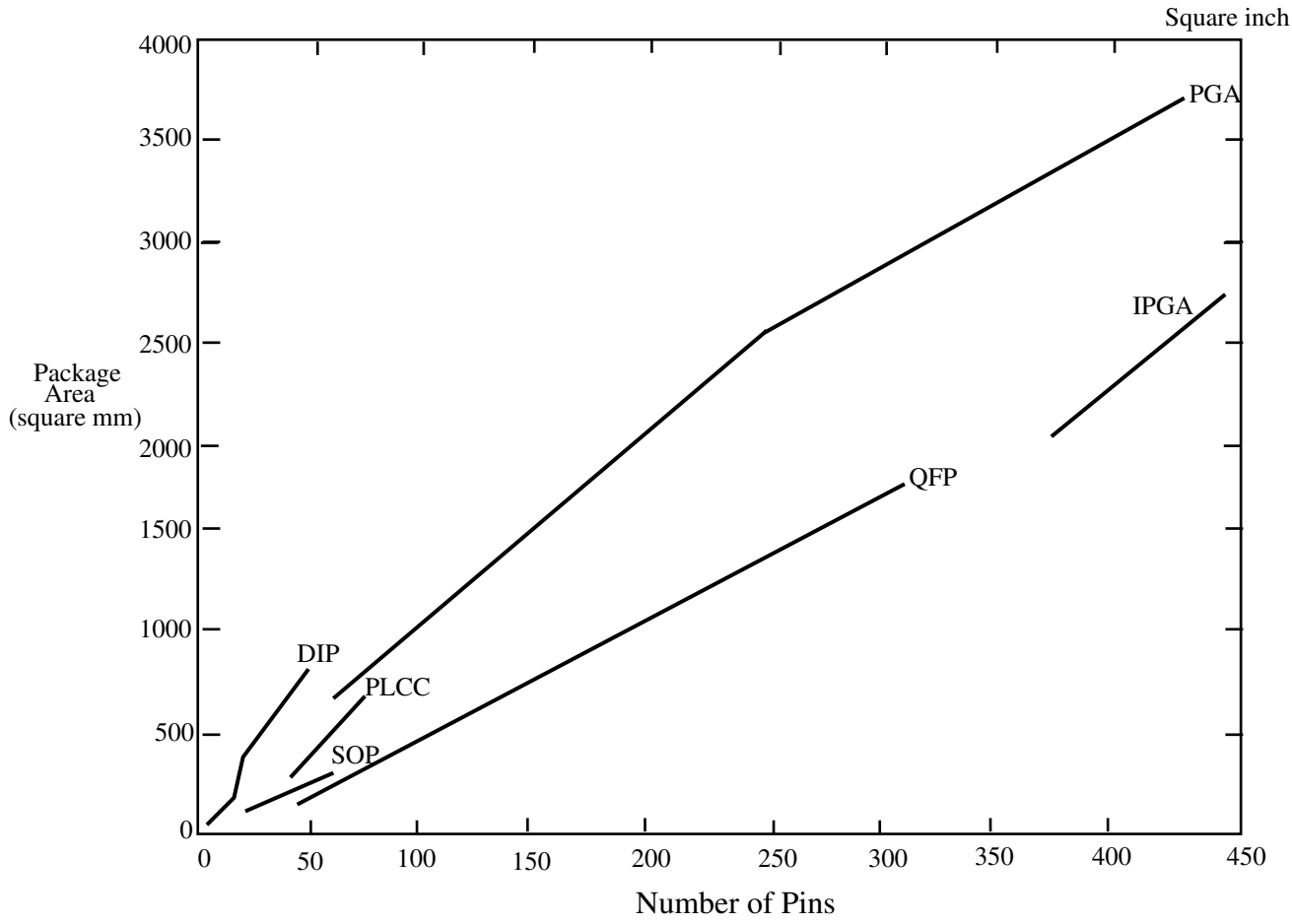
Figures 3-6 and 3-7 provide some general guidelines concerning package selection based upon power, frequency, pincount, and size.

Figure 3-6: Package Style Selection



Dashed lines indicate future trends.

Figure 3-7: Package Area versus Pincount



3.3.2 Through-hole Dual In-Line Package (DIP): Acceptable

According to A-PS-1900000-GS, the following attributes apply:

- Pin pitch is 0.100 inch.
- Pincount range is 8 through 40 pins. Higher pincount DIPs are to be avoided.
- Technologies include molded plastic (PDIP), MLC (CDIP), glass seal (CerDIP)

Preferred alternative is equivalent surface mount small outline (SO) package. (Refer to sub-heads 3.3.7, 3.3.8, 3.3.9, 3.3.10.)

Figure 3-8: Dual In-Line Package Outline

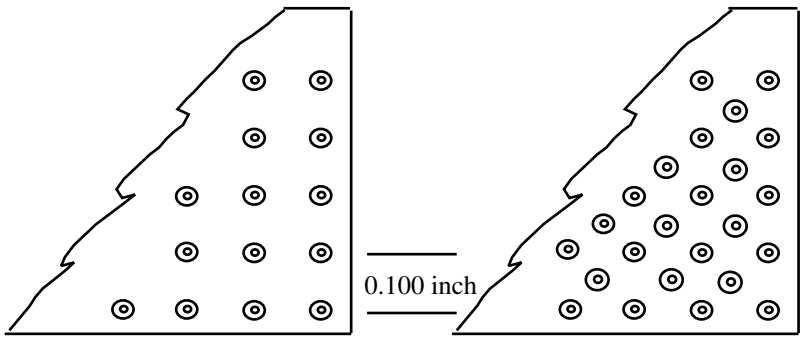
3.3.3 Through-hole Pin Grid Array (PGA) Package: Preferred

According to A-PS-1900015-GS and 1900019-GS, the following attributes apply:

- Pincount range is 68 through 431 in 0.100 inch full grid or up to 447 in 0.050 x 0.100 mil interstitial (IPGA) pattern.
- Technology is MLC.

These specifications only cover a subset of PGA packages; due to the custom nature of PGAs, it is necessary to refer to individual device purchase specifications for details on existing part types.

Figure 3-9: Pin Field Patterns, PGA and IPGA



0.100 inch PGA 0.100 x 0.050 inch Interstitial PGA

3.3.4 Surfacce Mount Cerquad: Acceptable

According to A-PS-1900034-GS the following attributes apply:

- Leadform is gull-wing.
- Technology is glass seal ceramic.

Preferred alternative is PQFP, where thermal requirements permit.

Table 3-3: Available Cerquad Packages

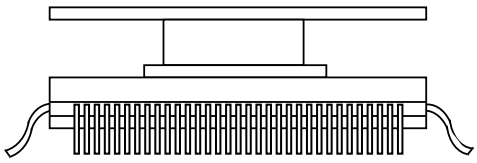
Pincount	Pin Pitch (inch)	Package Height (inch)	Package Footprint (inch)
44	.050	0.180/0.344	0.870 square
68	.050	0.180/0.344	1.170 square
84	.050	0.180/0.344	1.370 square
132	.025	0.180/0.344	1.170 square
164	.025	0.180/0.344	1.370 square

Notes:

Height is maximum dimension from seating plane to top of package without heat sink (first figure) and maximum dimension from seating plane to top of single platter heat sink (second figure).

Package Footprint is maximum dimension of PWB pad pattern.
These dimensions are for reference only. For the actual footprint to be used in a design, refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

Figure 3-10: Cerquad Outline



Package shown with permanent (glued) heat sink

3.3.5 Surface Mount Metric Plastic Quad Flat Pack (PQFP): Preferred

According to A-PS-1900023-GS the following attributes apply:

- Leadform is gull-wing.
- Technology is molded plastic.

Table 3-4: Partial Listing of PQFP Packages

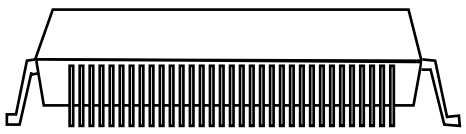
Pincount	Pin Pitch(mm)	Nom. Body Size (mm)	Package Height (mm)	Package Footprint (mm)
44	0.8	10	2.35	20.0 square
52	0.65	10	2.45	14.5 square
80	0.8	14x20	3.40	18.2 x 24.2
100	0.65	14x20	4.07	18.4 x 25.3
120/128	0.8	28	4.45	33.3 square
144	0.65	28	4.07	33.3 square
160	0.65	28	4.50	33.3 square
184	0.65	32	4.41	38.0 square
208	0.5	28	4.20	31.6 square
232	0.65	40	4.50	43.9 square
240	0.5	32	4.20	35.8 square

Notes:

Height is maximum dimension from seating plane to top of package.
Package footprint is maximum dimension of PWB pad pattern.
These dimensions are for reference only. For the actual footprint to be used in a design, refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

The U.S. semiconductor vendor base is supplying several English dimensioned PQFPs at 25 mil pitch. These are gradually being phased out.

Figure 3-11: PQFP Outline



3.3.6 Surface Mount Plastic Leader Chip Carrier (PLCC): Acceptable

According to A-PS-1900013-GS, the following attributes apply:

- Pin pitch is 0.050 inch.
- Pincounts over 84 pins are not acceptable.
- Leadform is J-Bend.
- Technology is molded plastic.

This English dimensioned format is being obsoleted by the metric PQFP, the preferred alternative.

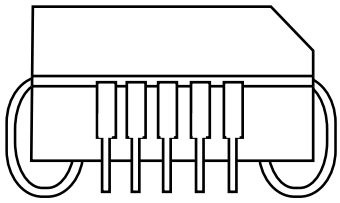
Table 3-5: Available PLCC Packages

Pincount	Package Height (inch)	Package Footprint (inch)
18	0.140	0.431 x 0.611
22	0.140	0.431 x 0.611
28	0.140	0.471 x 0.671
32	0.140	0.571 x 0.671
20	0.180	0.471 square
28	0.180	0.506 square
44	0.180	0.706 square
52	0.200	0.871 square
68	0.200	1.006 square
84	0.200	1.206 square

Notes:

Height is maximum dimension from seating plane to top of package.
Package footprint is maximum dimension of PWB pattern.
These dimensions are for reference only. For the actual footprint to be used in a design, refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

Figure 3-12: PLCC Outline



3.3.7 Surface Mount Small Outline J-Bend (SOJ): Acceptable

According to A-PS-1900032-GS the following attributes apply:

- Pin pitch is 0.050 inch.
- Leadform is J-Bend.
- Technology is molded plastic.

Preferred alternative is SOIC (Refer to subhead 3.3.7).

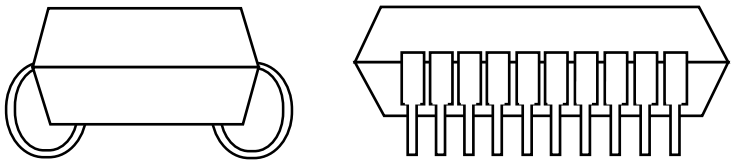
Table 3-6: Available SOJ Packages

Pincount	Package Height (inch)	Package Footprint (inch)
20	0.148	0.350 x 0.513
24	0.148	0.350 x 0.650
28	0.148	0.350 x 0.735
32	0.148	0.350 x 0.830
28	0.148	0.445 x 0.735
32	0.148	0.445 x 0.830

Notes:

Height is maximum dimension from seating plane to top of package.
Package footprint is maximum dimension of PWB pattern.
These dimensions are for reference only. For the actual footprint to be used in a design, refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

Figure 3-13: SOJ Package Outline



3.3.8 Surface Mount Small Outline IC (SOIC): Preferred

According to A-PS-1900017-GS the following attributes apply:

- Pin pitch is 0.050 inch.
- Leadform is gull-wing.
- Technology is molded plastic.

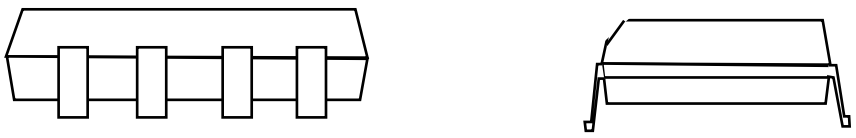
Table 3-7: Available SOIC Packages

Pincount	Nom Body Width (inch)	Package Height (inch)	Package Footprint (inch)
8	0.150	0.069	0.197 x 0.284
14	0.150	0.069	0.344 x 0.284
16	0.150	0.069	0.394 x 0.284
16	0.300	0.104	0.413 x 0.460
18	0.300	0.104	0.462 x 0.460
20	0.300	0.104	0.512 x 0.460
24	0.300	0.104	0.614 x 0.460
28	0.300	0.104	0.713 x 0.460
32	0.300	0.104	0.824 x 0.460
36	0.300	0.104	0.924 x 0.460
28	0.330	0.120	0.728 x 0.540

Notes:

Height is maximum dimension from seating plane to top of package.
Package footprint is maximum dimension of PWB pattern.
These dimensions are for reference only. For the actual footprint to be used in a design , refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

Figure 3-14: SOIC Package Outline



3.3.9 Surface Mount Thin Small Outline Package (TSOP): Acceptable

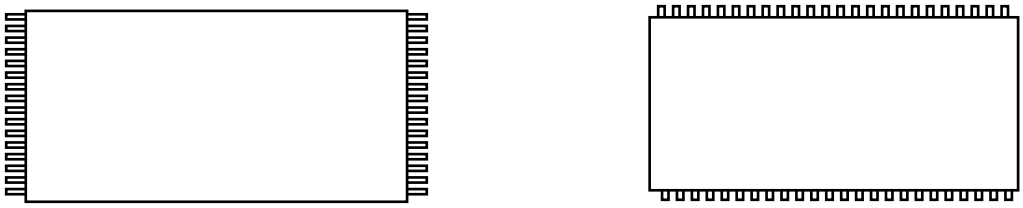
According to A-PS-1900046-GS and A-PS-2100008-GS the following attributes apply:

- There are two configurations: leads along the two short sides of the package (Type I) and leads along the two long sides of the package (Type II).
- Pin pitch is 0.5mm for Type I, 0.65, 0.80, and 1.27mm for Type II.
- Leadform is gull-wing.
- Various pincounts up to 40 pins.
- Technology is molded plastic.

The primary advantage of the TSOP is low body height for density in memory packaging, 1.20 to 1.27 mm (maximum). Currently, devices in these packages cost more (10% range) than the same device in the equivalent SOJ package. Thus, TSOPs should be used, at this time, only when the application dictates a low height package.

Some memory TSOP packages are offered in a reverse pincount configuration (mirrored for double-sided modules).

Figure 3-15: TSOP Type Differentiation Outline



3.3.10 Surface Mount Shrink Small Outline Package (SSOP): Acceptable

According to A-PS-1900045-GS the following attributes apply:

- Pin pitch is 0.025 mils.
- Leadform is gull-wing.
- Technology is molded plastic.

Table 3-8: Selected SSOP Packages

Pincount	Package Height (inch)	Package Footprint (inch)
48	0.095	0.630 x 0.434
56	0.095	0.730 x 0.434

Notes:

Height is maximum dimension from seating plane to top of package.
Package footprint is maximum dimension of PWB pattern. These dimensions are for reference only. For the actual footprint to be used in a design refer to KELVIN::[TECHFILES.FOOTPRINTS.TABLE].

Several lower pincounts are becoming available; the trend is to introduce the new pincounts in metric dimensions.

Figure 3-16: SSOP Package Outline

3.4 Trends

3.4.1 Dimensioning

Surface mount packages are moving toward metric dimensioning. through-hole (for example, PGA) will remain English dimensioned. Fine pitch array packages (< 2 mm pitch) will probably be metric dimensioned as standards emerge. These packages are expected to be surface mount types (refer to subhead 3.4.4, Ball Grid Array).

3.4.2 J-Bend Leadforms

J-Bend leadforms are gradually being discontinued by packages with gull-wing lead configurations. Parameters such as coplanarity and lead skew are more easily controlled in the manufacture of gull-wing packages, particularly in the finer (less than 0.050 inch) pin pitches

3.4.3 TSOP and SSOP Packages

TSOP and SSOP packages will become more prevalent and may dominate over the SOJ style in terms of preference for general application as well as memory. It is expected that the price disadvantage will disappear over time.

3.4.4 Emerging Package Configurations

This section highlights several emerging package configurations which show promise for future application within Digital. **None of these packages are included in T4.**

- Ball Grid Array (BGA) - a solder reflow surface mount array package. High pin density but locally coarse (as opposed to fine pitch perimeter leaded SMT types).
- Metal Quad (MQUAD) - similar to cerquad but in metric PQFP outline. Metal body for heat dissipation, epoxy (nonhermetic) seal.
- Enhanced PQFP (EPQFP) - same body and outline as the metric PQFP with electrical and thermal enhancements incorporated in the leadframe.

3.5 Multichip Packages

Multichip packages (those packages containing more than one active device) are acceptable as long as the package conforms to the dimensional and quality requirements of other LSI chip packages. The most common configuration is through-hole PGA.

3.6 Electrical Considerations

With a general trend, driven by improvements in chip level integration, toward higher pin-counts, faster operating frequencies, and increasing edge rates, the signal integrity aspects of IC packages are becoming increasingly important.

There are three areas of concern in selecting the suitability of a particular package technology or package design to a given chip. These are:

- Simultaneous switching (noise generated across the impedance of the power distribution interconnect when the IC draws transient currents during switching).
- Crosstalk (edge rate driven inductive and capacitive coupling between neighboring signal paths).
- Impedance and propagation delay of the signal paths.

All of the previously listed concerns are adversely impacted by the higher line densities and longer interconnect lengths that are the result of higher levels of silicon integration.

In the available set of package technologies, there are two broad categories of interest from an electical standpoint:

- Simple leadframe packages where the only design freedom is the allocation (number, location) of lines for a given purpose (for example, signal line, power or ground). As examples, signal lines may be placed between reference pins to reduce crosstalk and multiple power pins may be allocated to lower simultaneous switching induced noise.
- Multilayer ceramic packages where complex signal/reference structures may be built up.

As a general guideline, the leadframe based package is usually limited to a 30 MHz operating frequency for random logic devices. Multilayer structures of the type described in this chapter have been used to 85 MHz and should be extensible to over 250 MHz with no fundamental changes. In the case of low leadcount memory devices, increasing speeds and densities have had less of an effect: here packages are getting smaller (for example, the transitions from DIP to TSOP) and package interconnect has therefore remained less of an issue.

The details of the package selection and design for electrical performance are primarily the responsibility of the chip component supplier. Issues which are relevant to the module designer are covered in Chapter 11, Module Electrical Design of the Electronic Technology File. Details of the package electrical design process for Digital designed ICs are contained in the *SCO-SEG Packaging Technology and Design Guide*.

3.7 Thermal Considerations

The trend toward integrating and increasing functionality on silicon has resulted in increasing the power dissipation requirements of individual components. This has increased the need for greater awareness of thermal design and control issues associated with insuring the reliable performance of LSI/VLSI components.

3.7.1 Thermal Design and Control Considerations

Several variables affect the thermal performance and design of packages and heat sinks for individual components. These include :

- Junction temperature limits and ambient air temperature
- Air flow across the component
- Package construction, material and size
- Methods for attaching heat sinks to components
- Module assembly, placement, and reflow limitations

3.7.2 Junction Temperature Limits and Ambient Air Temperature

As prescribed in Chapter 12, Thermal Design (in process) and current Digital Standards, the following table outlines the junction temperature limits of individual components and the temperature of the ambient air surrounding entering the system enclosure.

Maximum Junction Temperature:	CMOS $\leq$ 85 C Bipolar $\leq$ 100 C
Max. Ambient Air Temperature: (According to DEC STD 102-0 *Environmental Standard for Computers and Peripherals - General Test Requirements*)	Class A - Computer Room Environment = 28C Class B - Office Environment = 35C Class C - Industrial Environment = 50C

Note:

The air temperature surrounding the component may be higher than the maximum ambient temperatures listed above.

3.7.3 Air Flow Across the Component

In general, the amount of heat transferred from a component increases as the air flow across the top of a component increases. The air flows across the components varies with system design and acoustic constraints. A table of typcial air velocities is as follows:

Table 3-9: Typical Air Velocities

Portables	No forced air - natural convection
Workstation/Desktop	0.5 to 1.0 m/s
Deskside/Copier	1.0 to 1.5 m/s
Small tower	1.0 to 2.0 m/s
Large Tower	2.0 to 5.0 m/s

3.7.4 Package Construction, Material and Size

How a package is constructed and the materials used can greatly affect the manner in which heat is transferred from the silicon to the air stream above the component. Thermal conductivity, thickness, cavity orientation and surface area are important package design considerations.

3.7.5 Methods for Attaching Heat Sinks to Components

Heat sinks can be attached to packages using one of two different methods currently in use. They can be 'permanently' attached using an epoxy/adhesive (the preferred choice for surface mount and low power designs); or a 'separable' type of design can be utilized whereby the heat sink is attached to the package using mechanical fasteners and can be removed or replaced if there is a need (recommended for high powered devices).

3.7.6 Module Assembly, Placement, and Reflow Limitations

Packages with heat sinks must be compatible with Stage 1 module assembly processes. This includes placement and reflow considerations.

PGAs are currently hand placed and assembled. Heat sinks attached to the these packages prior to reflow must not hinder this assembly and be compatible with the reflow equipment. Surface mount components that are machine placed and assembled require that heat sinks added to the components prior to reflow remain within the specifications of the placement equipment.

Table 3-10: Assembly, Placement, Reflow Requirement (Package with heat sink)

Specification	PGA/TH Requirements	Cerquad/SMT Requirements
Height of Package and heat sink	< 3 inch above the seating plane	< 0.400 inch above the seating plane
Maximum Footprint Dimensions of HS	not specified - must not affect assembly	not to overhang leads
Maximum Weight of Package w/heat sink	not specified	20 grams if HS Diam. > 25 mm 15 grams if HS Diam. < 25 mm (assumes platter HS)
Pick Up Surface Parallelism (w/HS)	not specified	not to exceed .008 inch
Pick UP Surface Flatness (heat sink)	not specified	.0015 inch

3.7.7 Thermal Modeling and Verification Testing

Several software tools are available for modeling the thermal performance of a package both with and without a heat sink. These tools are especially useful in solving complex 2D and 3D problems. For diffusion problems, ABAQUS and ANSYS are frequently used; while fluid flow analysis is generally more suited to tools like FLOWTHERM and FLUENT. There also exists several design guides and specific test data within the Corporation.

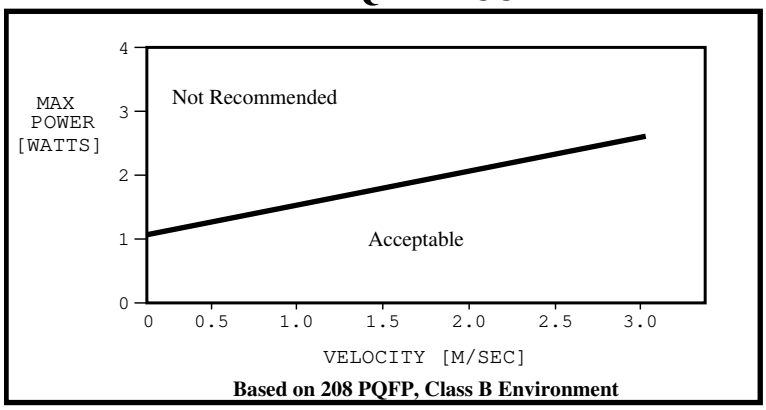
3.7.8 Package/Power/Heat Sink Selection

Omnidirectional or platter style heat sinks are the design of choice for permanently attached heat sinks affixed to packages prior to reflow. Because bidirectional or ribbed style heat sinks provide more surface area for a given volume they are generally the design of choice for higher powered designs and utilize a separable and mechanical heat sink attach method.

For guidelines in selecting packages based on thermal considerations, see Figure 3-17.

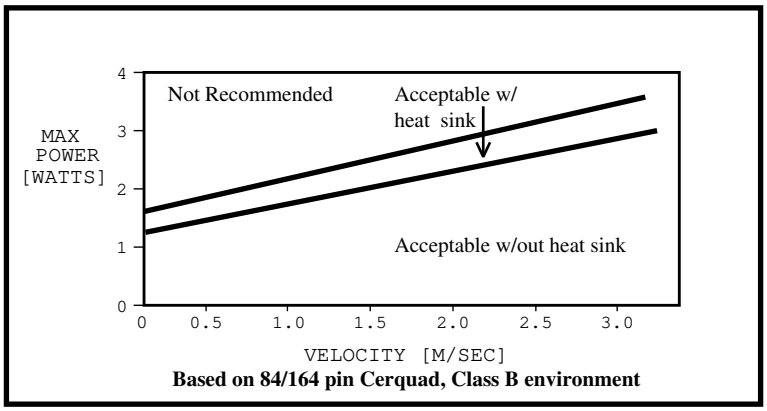
Figure 3-17: Package Thermal Performance

PQFP-PLCC



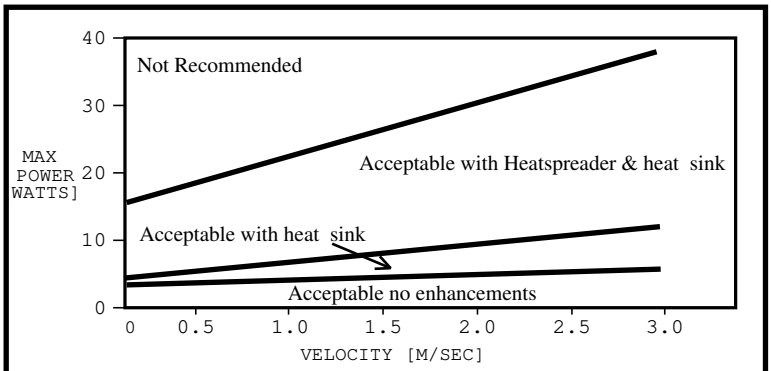
Based on 208 PQFP, Class B Environment

Cerquad



Based on 84/164 pin Cerquad, Class B environment

PGA



Based on 339 PGA with heat sink, 431 PGA with Heatspreader & heat sink, Class B Environment

3.8 Cost Considerations

Table 3-11 provides average industry cost data for packages of various styles and complexity.

Table 3-11: Industry Typical Assembled Package Cost

Package	Description	Average Cost
PLCC	Stamped copper, pins ≤ 84	$0.02
PQFP	Stamped copper, metric, pins ≤ 208	$0.02
Cerquad	25 and 50 mil, pins ≤ 144	$0.11
CPGA	Single layer, pins ≤ 144	$0.08
CPGA	3-4 layers, pins ≤ 304	$0.11
CPGA	> 4 layers, pins ≥ 304	$0.30

- Vendor preferences may skew actual costs.
- Assembled package cost is cost less die and does not include lids where applicable.
- Data from BPA, February 1992 except CPGA > 4 layers, which is from SCO/HLO Purchasing, October 1992.
- Stamped copper refers to lead frame material and production method.

In addition to the production costs given in Table 3-11, design costs may also be incurred if a new package design is required. Some typical design costs are given in Table 3-12 for selected packages. These costs are a consideration for internally produced chips and also for externally purchased chips when the package is a custom design. Furthermore, internally produced chips with new package designs may also require development of new die-into-package assembly process capability. Development of this capability may cost on the order of $50,000 to $500,000

Table 3-12: Package Design Costs

Package	Cost (in 1000s of dollars)	
	Minor Modification	New Design
Ceramic PGA	70	225+
Cerquad	40	100+
PQFP	50	275+

Notes for Table 3-12:

- Minor Modification: Same package body/pins as existing but new cavity.
- New Design: New package with new thermal and/or electrical performance features.
- Costs are based on internal SCO/SEG designs.

Finally, it should also be realized that the total cost impact of package selection can only be determined after a review of other associated product manufacturing costs such as board assembly.

3.9 Contributors

Major contributors to this chapter include the following:

Steve Hansen	TDA/Chapter Captain
Ken Brown	SCO/SEG
Scott Lorion	SCO/SEG
Eric Ren	SCO/SBO
Bob Brownwell	SCO/SBO
Ernie Allen	TDA/EPT
Steve Beckman	TDA/EMT
Joanne Mavroides	TDA/EMT
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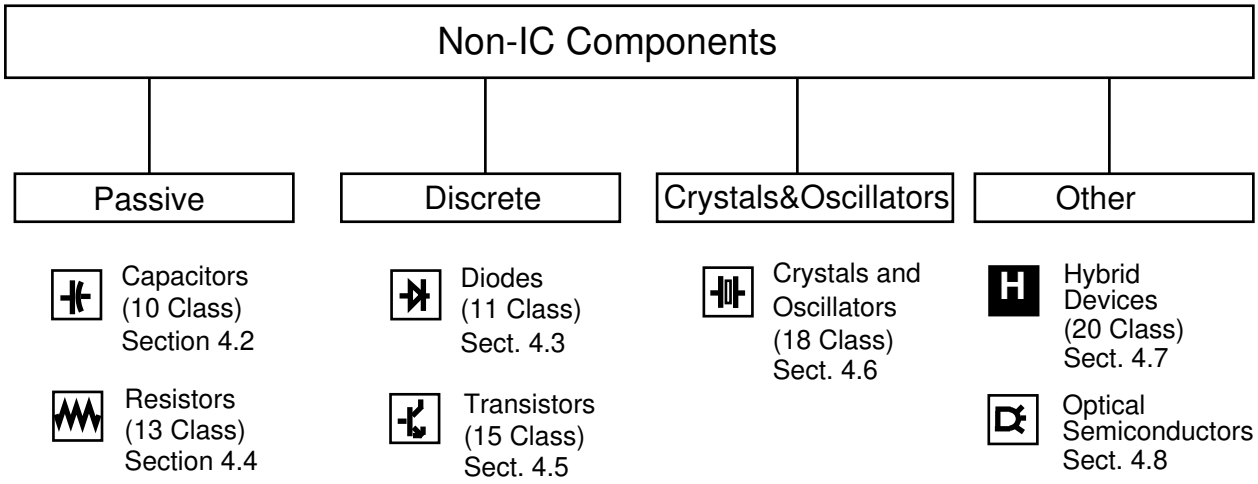
Chapter 4: Non-IC Components

4.1 Chapter Overview

This section covers the following component technologies. The first two digits in *Class* refers to the Digital part number.



Icons identify the sections of this chapter.

4.1.1 Chapter Team

The following people are responsible for the content of this chapter and may be contacted for additional information, design assistance, or suggestions for future additions to the chapter:

Name	Responsibility	DTN	E-mail
Don Brouillet	Chapter Captain	234-4696	GOLF::BROUILLET
George Checkowski	Crystal Oscillators	226-2840	LJOHUB::CHECKOWSKI
Jose Cruz	Resistors	244-7385	GIAMEM::CRUZ
John Funaro	Diodes Opto devices	226-2839	LJOHUB::FUNARO
Dennis Johnson	Hybrids	566-4039	DESERT::JOHNSOND
Roger Lachapelle	Transistors Crystal Oscillators	223-8046	LUNER::LACHAPELLE
Charles Lahaye	Capacitors	223-8061	LUNER::LAHAYE

4.1.2 Roadmap to Information Contained in This Section:

If you...

If you...		Refer to
Need to select the best technology for your application	→	Selection guides Subhead 4.x.1
Are familiar with the technology, and just need a quick reference to preferred parts	→	Preferred parts tables Subhead 4.x.2
Cannot find a preferred part to meet your needs, and/or need to know more details about applications, packaging, cost, reliability, and so forth	→	Design guide Subhead 4.x.3
Need more information than this chapter provides	→	Contact the appropriate chapter team member as shown in Subhead 4.1.1
Have comments, questions, or suggestions on the organization or content of this chapter	→	Contact the chapter captain listed in Subhead 4.1.1

Note: x in the reference corresponds to the subhead number for each device type as follows:

- Subhead 4.2 – Capacitors
- Subhead 4.3 – Diodes
- Subhead 4.4 – Resistors
- Subhead 4.5 – Transistors
- Subhead 4.6 – Crystals and Oscillators
- Subhead 4.7 – Hybrids
- Subhead 4.8 – Optical Semiconductors

4.1.3 Preferred Parts

Each subhead listed contains a quick-reference list of preferred parts. Whenever possible, these parts should be used if they meet the requirement of the application. The preferred parts tables

include *short form* data which, in most cases, will allow designers to find acceptable preferred parts, or at least identify the preferred technology for a given application.

Preferred parts represent the best choice for each technology from all of the existing Digital part numbers that are available for use in new designs. Preferred non-IC components are those that substantially meet the following criteria:

- Available now and in the future
- Compatible with manufacturing process
- Cost advantages
- Industry standard packages and devices
- Technical advantage, or the optimal choice from available parts
- Quality/reliability of technology and supplier

Widespread use of preferred parts for common applications will significantly reduce both cost and time in procurement, supplier management, inventory, and manufacturing set-up.

It is important to note that preferred parts will not meet every need. There are three categories of parts available. Listed in order of preference they are:

1. Preferred Parts—The optimal choice, to be used whenever possible. These parts are listed in the quick reference tables that follow.

2. Acceptable Parts—Values, ratings, packages, and so forth, that are not as widely applicable as preferred parts. Acceptable parts may be located by using Specifications on Computer (SPOC) or other component selection tools, using the guidelines established by the techfile.

3. Limited or Special Use—These parts are not generally available and are only used when unique application conditions prohibit the use of preferred or acceptable parts.

4.1.3.1 Changes to the Preferred Parts List

The Preferred Parts List (PPL) will be maintained by the individuals identified as the Techfile team for this chapter. The SPOC system is in the process of changing its preferred part identification and maintenance scheme to coincide with the Techfile. Requests for changes or additions to the Preferred Parts List should be channeled to the appropriate chapter team member.

4.1.3.2 New Parts

If no existing Digital part meets your needs, you will need to bring in a new part. Several components of the new part introduction process are being re-engineered to reduce cost and turnaround time. However, the process still requires several steps, including part number assignment, specification development, qualification, and supplier management. Costs can range from $500 to $10,000 for each new part introduced, not including the additional cost impact on manufacturing. Also, your project schedule may be substantially impacted by the time penalty incurred in bringing in new parts. For these reasons, and for the mutual benefit of all Digital concurrent engineering teams, designers are urged to contact the responsible component engi-

neer or the chapter team member listed in subhead 4.1.1 as early as possible if their project absolutely requires a new component technology.

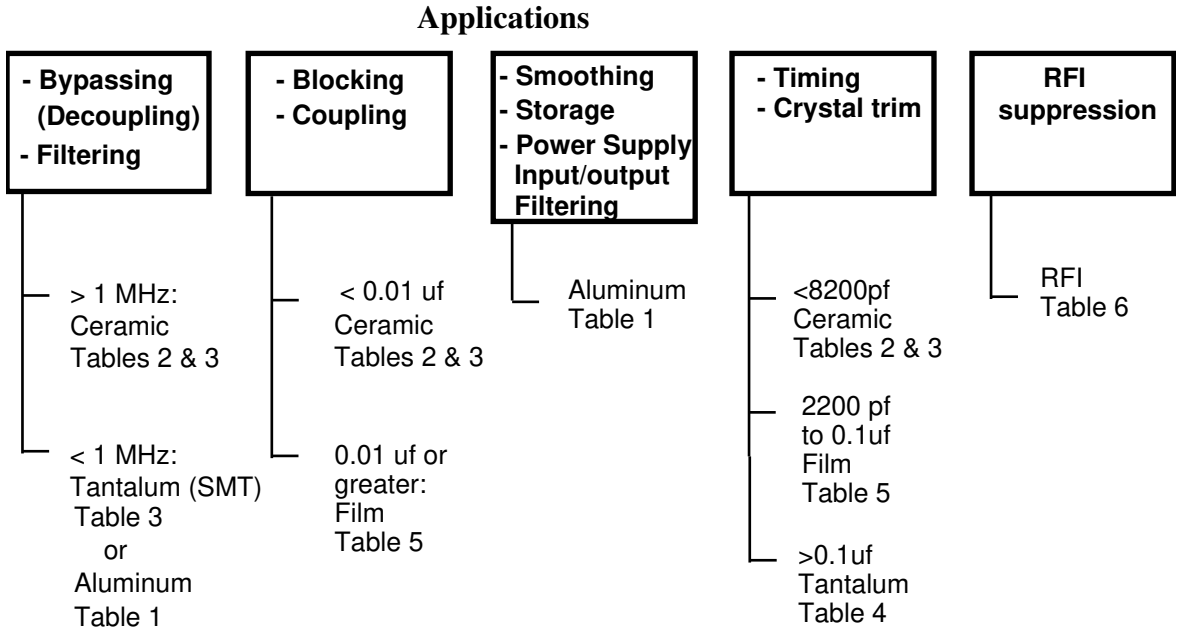
4.2 Capacitors

To select a capacitor follow these steps:

1. Select the appropriate technology by application.
2. Locate the preferred parts in the tables listed.
3. Refer to the design guide for further information if preferred parts do not meet the need.

Figure 4-1 outlines the capacitor selection procedure.

Figure 4-1: Capacitor Selection Guide



4.2.1 Capacitor Selection Guide by Application

Considerations by application are:

- Bypassing (Decoupling) or Filtering
  - — The primary consideration is to select a capacitance value that decouples a certain frequency. The ideal capacitor would provide a low impedance path around a given circuit. The preferred parts list shows four optimum ceramic capacitor values that will effectively decouple frequencies in the range from 500 kHz to 200 MHz.
  - — For low frequency bypass in the 50 kHz to 500 kHz range, select one of the preferred aluminum electrolytic capacitors. In surface mount designs, the only type of device currently available is the tantalum chip capacitor.

- Timing
  - — The primary considerations are stability over time and temperature, and close capacitance tolerance. Timing intervals of 1 second or less can use NPO ceramic or film capacitors. Timing intervals greater than 1 second require larger capacitance values that are found in tantalum capacitors.
  - — Most stable dielectrics are:
    - * NPO ceramic devices, available in SMT, axial, and radial-leaded packages
    - * Mylar or polypropylene film devices, available in leaded packages for through-hole assembly
    - * Tantalum electrolytic devices available in leaded packages and as surface mount chip capacitors
- Coupling
  - — Provides a low series impedance for transferring ac power or signals from one circuit to another. Primary capacitor characteristics suitable for coupling are low loss factor and low inductance.
  - — Most suitable dielectrics are:
    - * In ceramic devices, select an X7R or NPO dielectric. Available in leaded devices or surface mount chip.
    - * Mylar or polypropylene film devices available in leaded package for through-hole.
- Blocking
  - — Provides a high series impedance for limiting dc current flow. Primary capacitor characteristic suitable for blocking is high insulation resistance to dc current.
  - — Most suitable dielectrics are:
    - * In ceramics devices, select NPO, X7R, or Z5U dielectric.
    - * Mylar or polypropylene film devices available in leaded package for through-hole.
- Smoothing
  - — Smoothing or energy storage maintains the working voltage of the controlled circuit and suppresses transient voltages. The primary capacitor characteristics suitable for smoothing are good pulse and ac characteristics and low power loss.
  - — Most suitable dielectrics are:
    - * Aluminum electrolytic capacitors. These are best for input or output power supply applications. Aluminum capacitors are available in leaded packages for through-hole assembly.
    - * Tantalum surface mount chip capacitors are suitable for output smoothing of power supplies.

- Crystal trim
  - — Primary consideration is stability over time, temperature, and close tolerance.
  - — Most suitable dielectrics are NPO ceramic devices, available in SMT, axial, and radial-leaded packages.
- RFI suppression
  - — Primary consideration is safety and regulatory agency approval for use on ac power lines.
  - — Most suitable dielectrics are:
    - * Metallized mylar capacitors, available in leaded packages for through-hole assembly.
    - * Ceramic disk capacitors, available in leaded packages for through-hole.

4.2.2 Capacitor Preferred Part Tables

Table 4-1: Aluminum Electrolytic Capacitors (FCD AA, AR)

FCD/ Description	Application	Part Number	Capacitance (microfarads)	Voltage (volts)	Diameter (mm)	Length (mm)	Lead Space (mm)	Temp. (105°C unless indicated)	FY93 Std. Cost ($)
AA	Power supply	10-26872-01	22	100	11	23			0.18
Aluminum	filter	10-23313-01	47	15	9	20		85°C	0.21
Electrolytic		10-20446-13	100	25	9	20		85°C	0.04
Axial lead		10-25379-01	220	16	9	20	N/A		0.20
		10-26860-01	470	16	11	23			0.11
Selection limited		10-29673-01	1000	16	13	28			0.30
to use 105°		10-26532-01	2200	25	16	42			0.59
where available	Bulk bypass at module level	10-17472-00	10	35	5.5	14	N/A	85°C	0.042
AR	Power supply	10-26610-01	100	25	8.5	14	3.5		0.095
Aluminum	filter	10-34385-01	330	35	11	28	5.0		0.12 est.
Electrolytic		10-26575-01	470	50	17	28	7.5		0.25
Radial lead		10-34387-01	560	63	19	22	7.5		0.35
		10-22152-01	680	50	23	45	[3 pin*]		1.04
Selection limited		10-30931-01	1000	80	19	42	7.5		0.51
to use 105°		10-34277-01	2200	50	19	42	7.5		0.98
		10-30403-01	3300	35	19	38	7.5		0.53
		10-24423-01	4700	16	19	38	7.5		0.29
		10-35396-01	6800	63	36	42	10		2.24
	Power supply	10-35400-01	100	450	23	42	10		1.50
	input filter	10-33449-01	220	450	36	34	10		2.05
[* Refer to		10-26378-01	330	400	36	54	10		3.68
specification]		10-34805-01	470	450	36	54	10		4.07
		10-36465-01	1200	450	42	65	[5 pin*]		6.00

Table 4-2: Ceramic Leaded Capacitors (FCD AK, AJ)
Applications: Bypass, Coupling, Timing

FCD/ Description	Part Number	Optimum Frequency & Impedance at frequency f(MHz)/Z(mΩ)	Capacitance (microfarads unless labeled)	Voltage (volts)	Diameter (mm)	Length (mm)	Tolerance (%)	Dielectric	FY93 Std. Cost ($)
AK Ceramic axial lead	10-13466-19	100 / 250	470 pf	50	0.100	0.170	5	NPO	0.030
	10-13466-34	50 / 600	4700 pf		0.100	0.170	5	X7R	0.036
	10-12784-00	12 / 250	0.047		0.100	0.170	+80/-20	Z5U	0.022
	10-13466-11	4 / 40	0.22		0.130	0.400	+80/-20	Z5U	0.029
	10-29563-01	3 / 30	0.33		0.120	0.170	+80/-20	Z5U	0.058
	10-13466-01	For Timing Applications	10 pf		0.100	0.170	5	NPO	0.03
	10-13466-31		15 pf						0.026
	10-13466-02		18 pf						0.037
	10-13466-23		22 pf						0.025
	10-13466-04		33 pf						0.024
	10-13466-05		56 pf						0.024
AJ Ceramic radial lead					**Height/Thick**				
	10-18200-04	146 / 299	470 pf		0.200 / 0.125	0.200	5	NPO	0.038
	10-11740-01	50 / 400	3300 pf		0.200 / 0.125	0.200	10	X7R	0.038
	10-10978-32	10 / 200	0.047		0.300 / 0.150	0.300	10	X7R	0.042
	10-10274-01	6 / 25	0.22		0.390 / 0.125	0.200	+80/-20	Z5U	0.049

Table 4-3: Ceramic Surface Mount Capacitors
Applications: Bypass, Coupling, Timing

FCD/ Description	Part Number	Optimum Frequency and Impedance at frequency f(MHz)/Z(mΩ)	Capacitance (microfarads unless labeled)	Voltage (volts)	Package Size	Tolerance (%)	Dielectric	FY93 Std. Cost ($)
AS Ceramic chip surface mount	10-24051-21	266 / 72	470 pf		1206	5	NPO	0.025
	10-24052-10	93 / 187	4700 pf		1206	10	X7R	0.022
	10-24053-07	23 / 120	0.047		1206	20	Z5U	0.023
	10-24053-21	10 / 27	0.22	50	1206	20	Z5U	0.030
	10-24053-24	7.6 / 13	0.47		1210	20	Z5U	0.080
	10-24051-90	167 / 370	560 pf		0805	5	NPO	
	10-24052-31	60 / 628	5600 pf		0805	10	X7R	
	10-24053-06	19 / 125	0.047		0805	20	Z5U	
	10-24053-34	10 / 40	0.1	25	0805	20	Z5U	
Under-IC memory bypass	10-35915-01	13.6 / 57.8	0.1	50	1210	+80/-20	Z5U	0.045
For Timing Applications	10-24051-01	N/A	10 pf	50	1206	5	NPO	0.026
	10-24051-02		12 pf					0.026
	10-24051-03		15 pf					0.013
	10-24051-04		18 pf					0.026
	10-24051-05		22 pf					0.019
	10-24051-07		33 pf					0.033
	10-24051-09		47 pf					0.013
	10-24051-10		56 pf					0.026

Table 4-4: Tantalum Axial Lead Capacitors (FCD AC)
Applications: Timing

FCD/ Description	Part Number	Capacitance (microfarads)	Voltage (volts)	Diameter (mm)	Length (mm)	FY93 Std. Cost ($)
AC	10-02431-00	2.2	35	0.151	0.458	0.24
	10-05334-00	3.3	20	0.151	0.458	0.20
Tantalum	10-05306-00	6.8	35	0.151	0.458	0.196
axial lead	10-01476-00	10.0	35	0.305	0.858	0.56
	10-02433-00	22.0	35	0.305	0.858	0.44
	10-00079-00	47.0	20	0.305	0.858	0.48
	10-11605-00	100.0	10	0.305	0.858	0.60

Table 4-5: Tantalum Surface Mount Capacitors (FCD AT)
Applications: Bypass, Timing

FCD/ Description	Part Number	Capacitance (microfarads)	Voltage (volts)	Length (mm)	Width (mm)	FY93 Std. Cost ($)
AT	10-34976-16	4.7	25	0.248	0.138	0.18
	10-34976-22	10.0	35	0.299	0.182	0.22
Tantalum	10-34976-25	22.0	20	0.299	0.182	0.30
surface mount	10-34976-27	47.0	16	0.299	0.182	0.25
	10-34976-29	100.0	10	0.299	0.182	0.26

Table 4-6: Film Capacitors (FCD AG, AH)
Applications: Coupling, Blocking, Timing

FCD/ Description	Part Number	Capacitance (microfarads unless labeled)	Voltage (volts)	Length (mm)	Height (mm)	Thick-ness	Lead Space	Wire Size	FY93 Std. Cost ($)
AG	10-30155-03	2200 pf	100	0.293	0.264	0.103	0.197	0.022	0.046
Mylar Foil	10-30155-04	4700 pf	100	0.293	0.264	0.103	0.197	0.022	0.047
	10-30155-02	6800 pf	100	0.293	0.264	0.103	0.197	0.022	0.08
	10-26654-01	0.01	100	0.395	0.335	0.197	0.295	0.025	0.046
AH	10-30154-02	0.047	100	0.293	0.285	0.103	0.197	0.022	0.11
Metallized	10-20604-03	0.1	100	0.418	0.359	0.162	0.295	0.025	0.064
Mylar									

Table 4-7: RFI Suppression Capacitors (FCD AN)

FCD/ Description	Application	Part Number	Capacitance (microfarads unless labeled)	Voltage (volts AC)	Length	Height	Thick-ness	Lead Space	FY93 Std. Cost ($)
					(inches unless labeled)				
AN	X capacitors	10-34571-01	0.1		17.5 mm	15 mm	8.5 mm	15 mm	0.19
		10-34571-02	0.22		26 mm	17 mm	8.5 mm	22.5 mm	0.23
RFI		10-34571-03	0.33	250	31 mm	18 mm	10 mm	27.5 mm	0.28
suppression		10-34571-04	0.47		31 mm	20 mm	12 mm	27.5 mm	0.30
capacitors		10-34571-05	1.0		31 mm	27 mm	16.5mm	27.5 mm	0.60
	Y capacitors	10-32211-01	470 pf	400	0.394	0.394	0.315	0.300	0.08
		10-28920-01	1000 pf	250	0.590	0.590	0.197	0.375	0.19
		10-24375-01	2200 pf	400	0.827	0.512	0.276	0.650	0.15
		10-24375-02	3300 pf	250	0.827	0.515	0.256	0.650	0.15
		10-35398-01	4700 pf	250	12 mm	12 mm	4.5 mm	7 mm	0.26
		10-24375-03	4700 pf	250	0.827	0.571	0.295	0.650	0.18

4.2.3 Capacitor Design Guide

Table 4-8 shows the different capacitor technologies available. A brief description of each and specific design and application data follow the table.

Table 4-8: Capacitor Technology Comparison Matrix

FCD	Technology	Application	Cost	Assembly Notes	Reliability Considerations	General Specification
AA	Minimum aluminum electrolytic 1µF–5000 µF	Bypass	0.04 / 0.25 / 1.59	Auto insert (through-hole) up to 0.2 inch dia. Manual assembly for larger sizes	Use 105° parts for best reliability	10- 00100-GS
AB	Large aluminum electrolytic	Bypass	1.00 / 3.50 / 16.00	Manual - screw mounted	Limit case temp rise to 20°C	10- 00102-GS
AR	Radial mount Aluminum electrolytic	Bypass	0.05 / 0.20 / 9.50	Manual assembly	Use 105°C parts for best reliability	10-00101-GS
AK	Ceramic axial lead 3.3pf–0.47µF	Timing coupling bypass	0.02 / 0.10 / 0.58	Auto insert (through-hole)	Derate voltage by 50%	10-00103-GS
AJ	Ceramic radial lead 12pf–1µF	Timing coupling bypass	0.02 / 0.15 / 1.00	Manual assembly	Derate voltage by 50%	10-00104-GS
AS	Ceramic chip surface mount 4.7pf–1µF	Timing coupling bypass		SMT	Chip size	
AC	Minimum tantalum polarized 0.47–270µF	Timing	0.21 / 0.35 / 3.87	Auto insert up to 0.21 inch diameter	Use FCD AA for bypass (miniature aluminum)	10-00002-GS
AT	Tantalum chip surface mount high frequency General Purpose 1–150µF	Timing bypass	0.21 / 0.50 / 0.75 0.12 / 0.20 / 0.33	SMT	Derate voltage by 50%	10-00106-GS
AE	Ceramic disk radial lead 5.2pf–0.1µF	Timing bypass Use FCD AK for <100V apps	0.01 / 0.06 / 0.76	Manual assembly	Derate voltage by 50%	
AD	Mica dipped radial lead 5–6800pf	Timing Use FCD AK for <100V apps	0.06 / 0.15 / 0.83	Manual assembly	Derate voltage by 50%	10-00003-GS
AG	Non-metallized mylar film 2200pf–1µF	High pulse current	0.04 / 0.25 / 0.80	Auto insert up to 0.2 inch diameter	Derate voltage by 50%	10-00001-GS

4.2.3.1 Aluminum Electrolytic Capacitors (FCD AA, AB, AR)

- Characteristics

The dielectric in this type of capacitor consists of a thin film of aluminum oxide. Electrolytic capacitors, unlike most other capacitor systems, contain an electrolyte system. Most electrolytes are wet systems. This electrolyte is impregnated into the paper separator between two wound foils of aluminum. The capacitor assembly is packaged in an aluminum can and covered with a plastic sleeve.

Aluminum electrolytic capacitors are not available in surface mount (SMT) packages at this time. They are available in axial or radial leaded packages, or, for large values, in a cylindrical package with screw terminals. Axial styles, which consume more PWB space than the vertically mounted radial lead devices, are generally used only when space is not a prime consideration.

- Packaging

The standard package style is a cylindrical package with axial leads (AA), radial leads (AR), or, for large devices, screw terminals (AB). User trends are to avoid the axial style which consumes more space than vertical mount aluminum capacitors. The single-ended version tends to have greater volumetric efficiency than the axial style.

- Assembly Implications
  - — Process sensitivity: Detergent-water clean only. Aluminum electrolytic capacitors shall not be subjected to immersion or vapor cleaning or any form of testing using halogenated hydrocarbon solvents. Case temperature should not be allowed to exceed 100°C during wave solder process.
  - — Placement: Axial and radial-leaded capacitors should not be placed over plated through vias on the modules.
  - — Screw terminal attachment: Assembly to modules or bus bars is accomplished by the use of screws, using a maximum torque of 8 inch-pounds.
- Electrical Design
  - — Voltage range varies from a low of 6.3 volts to a high of 450 volts. Voltage capability is inverse to the capacitance value. This characteristic is not linear, that is, with the higher voltage devices, the ratio of capacitance to voltage rating is smaller.
  - — Safe operating area is at approximately 80% of marked voltage rating and at the maximum ambient temperature rating for the specific device.
  - — Maximum ripple current limits shall be the value specified for the specific part as defined in the general specification. This ripple current should be at a level where the temperature of the capacitor case shall not be more than 15° above ambient temperature.
  - — Polarity: Aluminum electrolytic capacitors are polarity sensitive and will fail if installed with reversed polarity.
  - — Equivalent series resistance (ESR) decreases with increasing frequency above the 120 Hz standard measurement frequency.

- Thermal Design Considerations
  - — Temperature rating: There are two standard maximum operating temperature limits for aluminum electrolytic capacitors, 85°C and 105°C. Whenever they can be used, 105°C devices are preferred.
  - — Radiating heat sources such as heat sinks, power resistors, and high power semiconductors should not be located any closer than 1 inch from the aluminum capacitor.
  - — Temperature characteristics of capacitance is approximately a 10% increase at maximum temperature when compared to room temperature ambient. Approximately a 40% capacitance loss will occur at -40°C. ESR will decrease approximately 30% with a temperature at maximum ambient temperature.
- Reliability Considerations
  - — Storage: Aluminum electrolytic capacitors deteriorate during storage. The deterioration is temperature dependent; the higher the temperature the faster deterioration proceeds. Aluminum electrolytic capacitors should not be stored for more than two years at room temperature. Devices stored at temperatures greater than room temperature, or for longer periods of time, should be subjected to a voltage treatment which reforms the dielectric. Failure to do so could cause the capacitor to vent or severely shorten capacitor life.
  - — Deep charge and discharge cycles greater than 10% of the application voltage could increase failure rate by as much as 50 times or may even result in vented (failed due to overpressure) capacitors.
  - — Initial Failure Modes: The initial failures are generally catastrophic in nature. These failures show up as short circuits and are caused by manufacturing or material defects.
  - — Wearout Failure Mode: Unlike most electronic devices, electrolytic capacitors exhibit wearout, due to loss of electrolyte over time. The wearout failure mode is parametric degradation. The capacitance decreases by 20% and the ESR or dissipation factor doubles. End of life is usually an open capacitor.
  - — Acceleration factors are operating temperature and voltage stress. Each 10° reduction in operating temperature will reduce the the failure rate by half. Reducing the application voltage to 80% of rated voltage will reduce the failure rate by approximately 70%.
  - — A design hint for long life and acceptable reliability is to operate at a maximum of 80% of rated voltage and at the lowest possible temperature. Never exceed the maximum temperature as defined in the purchase specification.
- Cost factors
  - — Cost varies with case size. The larger the product of capacitance times the voltage, the higher the cost.
  - — Cost sensitive parameters are:
    - * Nonstandard capacitance value
    - * Special insulating sleeve other than polyvinyl chloride

* Nonstandard lead lengths

— Large tubular devices, FCD AB, are the least automated of any of the aluminum electrolytic capacitor styles. Consequently, they carry the highest cost per microfarad.

- Alternatives

When module height is not a restriction, consider the use of the vertical mount style aluminum electrolytic capacitor. The vertical mount style is found under FCD AR.

- Trends
  — The industry trend is to provide higher capacitance and voltage ratings in smaller case sizes.
  — Aluminum electrolytic capacitors are considered a mature product. Continuous product improvements are expected, such as increased volumetric efficiency resulting in smaller sizes.
  — Cost trend indicates the price will remain flat over the next 2 to 3 years.
  — Growth will take place only in vertical mount devices, because designs have switched from axial styles to reduce consumption of module space.

4.2.3.2 Ceramic Capacitors [FCD AU, AJ, AK]

- Characteristics

The dielectric in this type of capacitor is ceramic. The dielectric is cast in thin sheets; metal electrodes are deposited onto the thin sheets which are then stacked to form a laminated structure. The ceramic dielectric is available in several compositions. The principal dielectrics used in Digital products are NPO, X7R, and Z5U. The standard voltages range from 25 V to 200 V. Special designs with voltages up 5 kV are possible. The capacitor stacks can be packaged in glass case, epoxy conformal coating for leaded devices, or in a bare chip for surface mount requirements.

- Dielectrics

Ceramic dielectrics are designated by industry standard codes. The three most commonly used dielectrics, and the meaning of the three-character designation, are shown below.

Dielectric	Δ Capacitance Over Temperature Range	Temperature Range	Applications			
			Bypass	Timing	Coupling	Blocking
NPO	0 ± 30 ppm	-55°C to +125°C	X	X	X	X
X7R	± 15%	-55°C to +125°C	X		X	X
Z5U	+22% — 56%	+10°C to + 85°C	X			X

- Packaging

The standard package styles are radial lead (AJ), axial lead (AK), and bare chips (AS) for surface mount. The size varies, increasing in size with increasing capacitance and voltage. The surface mount capacitors are available in standard EIA sizes 0805, 1206, 1210, 1812, and 1825.

- Assembly Implications
  - — Process sensitivity: The radial lead and axial lead ceramic capacitors are through-hole mounted components processed in a wave solder applied to the bottom of the module. Surface mount assembly in vapor phase or IR is the least problematic. Several major issues occur in side 2 applications. One issue is that when chip ceramics are to be subjected to wave solder, the maximum temperature delta between preheat and the solder temperature shall be 100°C. Ceramic chip capacitors for use on side 2 applications should avoid the larger sizes of 1812 and 1825.
  - — SMT package: The conditions of the surface mount process require the terminations of the ceramic chip capacitors to be supplied with a nickel barrier with a tin/lead or pure tin coating.
  - — Placement: The radial lead capacitors are designated for hand insertion resulting in higher assembly cost. The axial style capacitors are inserted by machine resulting in lower assembly cost. The surface mount style component is intended for direct attach to pads on a printed module using solder paste and a solder reflow process. Surface mount chip ceramic may also be attached to side 2 of a module using an adhesive and then processed through wave solder.
- Electrical Design
  - — Standard voltage range varies from a low of 16 V to 200 V. Special voltages up 5000 V may also be available.
  - — Safe operating area is approximately 50% of marked voltage rating and at the maximum ambient for the specific dielectric in question.
  - — Polarity: Ceramic capacitors are not polarity sensitive and may be oriented in any direction.
  - — In inductance bypass applications the axial lead ceramic capacitor has the highest inductance of 3.0 nanohenries when mounted on 0.300 inch centers. The radial lead ceramic has a inductance of 1.8 nanohenries mounted on 0.200 inch centers. The ceramic chip has a nominal inductance of 1.4 nanohenries.
  - — Effects of voltage: Variations in voltage affect the capacitance and the dissipation factor. Each of the three dielectrics behave in a different way with voltage applied. NPO dielectrics are the most stable; capacitance and dissipation factor are unaffected by voltage stress. X7R dielectrics exhibit a negative coefficient of capacitance with increasing dc voltage. Minus 10% at rated voltage is typical. Z5U dielectric exhibits the largest coefficient of capacitance with increasing dc voltage. Minus 30% rated voltage is typical.
- Thermal Design Considerations
  - — Temperature rating: Each of the three dielectrics have different temperature ranges depending on the particular dielectric. NPO and X7R systems operate over the same temperature range of –55°C to maximum of 125°C. Z5U dielectric operating range is from +10°C to +85°C.
  - — Temperature characteristics: Capacitance changes with temperature vary with the dielectric. Over the temperature range listed the three dielectrics will exhibit the following capacitance change:

  * NPO: ± 30 parts per million
  * X7R: ± 15%
  * Z5U: +22% to –56%

- Reliability Considerations
  — Storage: Ceramic capacitors do not have any severe long term shelf storage issues. Leaded devices may develop soldering problems when subjected to storage in excess of 1 year in high humid climates. Capacitance of the X7R and Z5U will degrade when stored for very long periods. This condition can be reversed by de-aging the capacitors, which will restore the capacitance value.
  — Initial Failure Modes: The initial failures are catastrophic in nature. These failures show up as short circuit of low insulation resistance and are generally caused by thermal cracking during the Digital manufacturing solder process at the module level.
  — Wearout Failure Mode: The failure mode at end of life is also catastrophic which shows up as severe degradation of insulation resistance to a low value.
  — Acceleration factors: Acceleration factors are operating temperature and voltage stress. Each 10° reduction in operating temperature will reduce the failure rate by half. The voltage acceleration is the ratio of rated voltage over the operating voltage raised to the fifth power.
  — Design hints: For long life and acceptable reliability operate the capacitors at a maximum of 50% of rated voltage and at the lowest possible temperature.

- Cost Factors
  — Cost varies with capacitance and voltage. Higher capacitance values and higher voltage result in higher cost.
  — Cost sensitive parameters are:
    * Nonstandard capacitance value
    * Nonstandard lead cut
    * Special marking
    * Special lead form

4.2.3.3 Tantalum Electrolytic Capacitors [FCD AC,AT]

- Characteristics

The dielectric in a tantalum electrtolytic capacitor consists of a thin film of tantalum pentoxide. Electrolytic capacitors, unlike most other capacitor types, contain an electrolyte system. The electrolyte used in these capacitors is manganese dioxide and is, in effect, the cathode plate of the capacitor system. Tanatalum capacitors are available in surface mount packages and in through-hole versions in both axial or radial style packages.

- Packaging

  — The standard packages for through-hole versions are:

    * Axial leads (AC) with a cylindrical case

* A radial style finished in teardrop shape epoxy coating

— Surface mount versions (AT) are a basic chip style finished with a conformal epoxy coating or a molded epoxy case.

- Assembly Implications

— Process sensitivity: Detergent-water cleaning or solvent-vapor cleaning are suitable for tantalum leaded style and surface mount style. Case or lead of leaded types should not be allowed to exceed 150°C during wave solder process. Surface mount tantalum style are limited to a maximum temperature of 260°C for 10 seconds.

— Placement: The radial lead tantalum capacitors are designated for hand insertion resulting in higher assembly cost. The axial style tantalum capacitors (up to 0.2 inch diameter) are inserted by machine resulting in lower assembly cost. The surface mount style tantalum component is intended for direct attach to pads on a printed module using solder paste and a solder reflow process. Surface mount tantalum chip capacitors may also be attached to side 2 of a module using an adhesive, and then processed through wave solder.

- Electrical Design

— Voltage range varies from a low of 4 volts to a high of 125 volts. Voltage capability is inverse to the capacitance value.

— Safe operating area is approximately 80% of marked voltage rating and at maximum ambient temperature rating for the specific device. Most tantalums are specified at a maximum temperature of 85°C, however they may be operated up to 125°C by derating the rated voltage by two-thirds.

— Polarity: Tatalum capacitors are polarity sensitive and will fail if installed with reverse voltage. The maximum reverse voltage allowed is 10% of the rated voltage.

— Reverse voltage applications: It is permitted to connect two tantalum capacitors (cathode to cathode) to effectively create a nonpolarized capacitor. Each capacitor in the series connection has to be twice the final value required.

— ESR decreases with increasing frequency. The 100 kHz resistance value is indicated for each part in the general specifications (10-00106-GS and 10-00002-GS).

— Surge current: Tantalum capacitors are susceptible to high inrush currents. Peak inrush currents greater than 7 amperes may cause tantalum capacitors to fail in a short circuit mode. The normal turn on sequence of a system/power supply surge current is not sufficient to harm the tantalum capacitor.

- Thermal Design Considerations

  — Temperature rating: The maximum operating temperature limit for tantalum electrolytic capacitors is 125°C. Tantalum capacitors can be applied at rated voltage up to 85°C and derated to two thirds rated voltage at 125°C.

  — Radiating heat sources such as heat sinks, power resistors, and high power semiconductors should not be located any closer than one-half inch from the tantalum capacitor.

  — Temperature characteristics of capacitance is approximately a 10% increase at 125°C when compared to room ambient. Approximately a 5% loss of capacitance occurs at –40°C.

- Reliability Considerations

  — Storage: Solid tantalums exhibit very small electrical parametric deterioration during storage. Parametric characteristics are stable for greater than 10 years at storage temperatures less than 40°C. Long term storage will impact solderability, however.

  — Failure mode: In low impedance circuits failures are generally catastrophic in nature. These failures show up as short circuit and are caused by manufacturing or material defects. In high impedance circuits, failure is generally parametric in nature. The time span required for the parametric drift will generally exceed a product life of 10 years.

  — Failure rate: The failure rate of the solid tantalum capacitor decreases over time with voltage and temperature stress.

  — Derating: Operating at 60% of rated voltage will reduce failure rate by approximately 10 times. The minimum recommended derating is 80% of rated voltage.

- Cost factors: Cost varies with case size; the larger the product of capacitance times the voltage, the higher the cost.

  — Cost sensitive parameters are:

    * Nonstandard capacitance values

    * Non-E.I.A. standard case sizes

    * Surge current testing

- Alternatives: For any bypass applications, the preferred selection should always be a capacitor selected from the aluminum electrolytic series in FCDs AA and AR.

- Trends

  — Industry trend: The industry trend is to provide higher capacitance values in the current case sizes in the surface mount style. Cost is higher for the extended capacitance values.

— Maturity: Tantalum capacitors are considered a mature product. Continuous product improvements are expected, such as reduced ESR for the general purpose tantalum.

— Cost trend: The through-hole style price is at bottom levels. The surface mount tantalum price will tend to decrease as volume and capacity increases.

— Growth: Growth will take place only in the surface mount devices, because designs have switched from axial styles in order to reduce consumption of module space. The demand for higher frequency performance has been a significant force in the switch to surface mount styles.

4.3 Diodes

This section discusses the types of diodes and related devices listed in Table 4-9.

Table 4-9: Types of Diodes

FCD CODE	DESCRIPTION
BA BN	Zener diodes Zener diodes, SMT
BB	Rectifiers
BC BR	Switching diode Switching diode, SMT
BE BE1	Voltage transient suppresser Voltage transient suppresser, SMT
BF	Diode/Rectifier assemblies
BG BG1	Small signal diode arrays Small signal diode arrays, SMT
BH	SCRs, TRIAC's
BI	PIN diodes
BJ BJ1	Ultra-fast rectifiers Ultra-fast rectifiers, SMT
BM BM1	Schottky Diodes Schottky Diodes, SMT

4.3.1 Diode Selection Guide

- See Table 4-9 for the desired device type.
- Review selection criteria below before choosing a particular device or package.
- See subhead 4.3.1.2, Diode Selection Process for details on certain parameters.
- Find preferred parts in tables beginning on page 4-24.

4.3.1.1 Diode Selection Criteria

Questions to consider:

- What technology is needed: diode rectifier, rectifier assembly, switching diode/array, voltage transient suppressor, ultra-fast or Schottky diode (for high frequency application), or SCR/Triac?
- What type of package: surface mount or through-hole?
- Low frequency with long transition times or high frequency with fast transition times?
- Any parameters with tolerances/minimum-maximum limits?
- Any special space, cost, or reliability constraints?

Hints to minimize cost include:

- Select the lowest reverse voltage rating/lowest forward current and/or total power dissipation that can be used in the application.
- Avoid tight tolerance devices.
- Surface mount parts are generally preferred.

4.3.1.2 Diode Selection Process

Detailed steps for selecting the right device, by technology, are given below. It is important to note that the short form data for preferred parts or families in this section is not a complete specification. The most important characteristics are indicated. In the majority of cases, this will allow choice of a preferred part or family of parts needed for the application. The selected part number, GS specification (Digital General Specification), and FCD code can then be used to access additional data or complete specifications and qualified vendors using SPOC.

4.3.1.3 Steps in Selecting a Zener Diode

In general, the approximate value of the voltage to be regulated and its required tolerance is known and final selection should be made from the Preferred Parts List after the following circuit/device requirements are established:

- The maximum and minimum values of current to flow through the zener diode should be calculated from circuit needs. Zener power dissipation should be approximated from PDZ = VZ * IZmax. Choose the standard zener power rating from Table 4-26, FCD=BA, BN that is equal to or the next higher power rating to the required power rating.
- What type of package is required—surface mount or through-hole (many recent modules require all surface mount components)? Knowing the power dissipation and the package style, refer to the Preferred Parts List and obtain the general specification for the part family required.
- Review the total specification for the device chosen. (It should be the part listed in the Preferred Parts List with the nominal voltage required and the largest tolerance listed that will meet the application needs.)
- After device selection, recalculate PDZ using PD = (VZ nominal + tolerance) * (IZ max) to be certain that maximum power dissipation rating is not exceeded.
- Calculate zener voltage worse case using VZ ± tolerance at IZ minimum, maximum. (Note that this may have to be calculated by extrapolation of $\Delta VZ = ZZT$ (IZ max) + VZ nominal. The temperature coefficient (TC) of the zener voltage will also have to be calculated and added to this zener voltage: $\Delta VZ(TC)$ = operating temperature * MV/°C.

4.3.1.4 Selecting a Rectifier, Rectifier Assembly, Ultra-Fast Diode, or Schottky Diode

Consider the following issues to select a diode:

- If the application is low frequency, then use a rectifier. If it is high frequency, use an ultra-fast or Schottky diode to minimize reverse switching losses.

- Select the device technology (FCD) by the application requirements and reviewing Table 4-26. If the application requires more than one device, consider multiple devices (2 or more diodes in one package such as common cathode device in TO220 package) or single phase bridges (4 diodes in a bridge configuration). These devices are usually lower in price than the equivalent number of individual parts and also offer cost savings in manufacturing (inventory, placement/assembly) of one part rather than multiple parts.
- Select device technology (FCD) in Table 4-26 by:
  - — High or low frequency as indicated by reverse recovery time (trr)
  - — Power/current rating
  - — Voltage rating
- In high frequency applications, reverse switching losses can be higher than forward conduction losses. Reverse losses = PRAV=f*VR(QF+IR-TR) where f = frequency, QF = charge recovered during trr, tr=time VR applied. Junction temperature (operating) must be lower than maximum rating.

  Tj (opr) = Tcase or Tlead + Ptotal *Rθj-c OR
  Tj (opr) = Tambient + Ptotal *Rθj-c
- Schottky barrier diodes offer the highest efficiency in high frequency applications because forward conduction is lower than PN junction diodes. Switching losses are lower because of minimal trr since this part is a majority carrier device.

4.3.1.5 Steps in Selecting a SCR

- Select the maximum voltage rating and the maximum current rating of the mains diode.
- Select for package type—plastic type preferred.
- Select for maximum dv/dt if device is to switch alternating current.
- Select for correct gate trigger voltage.
- Select for correct gate trigger current and gate holding current.

4.3.1.6 Steps in Selecting a TRIAC

- Select the maximum voltage rating and the maximum current rating of the mains diode.
- Select for package type—plastic type preferred.
- Select for proper quadrants of conduction.
- Select for proper gate trigger voltage.
- Select for proper gate trigger current and gate holding current.

4.3.2 Diode Preferred Parts Tables

Table 4-10: Zener Diodes, Axial Leaded (FCD BA)

Part Number	Voltage (volts)	Tolerance (%)	Power (MW)	FY93 Std. Cost ($)	Cost trend	AVL Vendor
11-04860-00	3.3	5	400	0.0225	Flat	Motorola
11-05871-00	5.15	1	250	0.0600		
11-10856-00	24	5	400	0.0225		
11-24037-01	36	5	400	0.0225		
11-09502-00	12	10	1000	0.0350		
11-05648-01	15	5	1000	0.0350		

Table 4-11: Zener Diodes, Surface Mount (FCD BN)

Part Number	Voltage (V)	Tolerance (%)	Power (MW)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)
11-25346-09	5.1	5	260	0.0580	Down	Motorola/ Philips
11-25346-10	5.6	5	260	0.0580		
11-25346-11	6.2	5	260	0.0580		
11-25346-12	6.8	5	260	0.0580		
11-25346-14	8.2	5	260	0.0580		
11-25346-15	9.1	5	260	0.0580		
11-25346-16	10.0	5	260	0.0580		
11-25346-18	12.0	5	260	0.0580		
11-25346-20	15.0	5	260	0.0580		
11-34637-02	5.1	1	260	0.350		Motorola

Table 4-12: Rectifiers, Axial Leaded (FCD BB)

Part Number	Voltage (V)	Current Rating (Amps)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-05796-00	400	1	0.021	Flat	General Instrument (GI)	-	DO41
11-16474-00	400	1	0.022			-	DO41
11-25532-01	400	3	0 .110			-	DO201
11-25532-02	600	3	0.110			-	DO201
11-25268=01	200	1	0.045			150	DO41
11-25268-02	50	1	0.045			150	DO41
11-25268-03	100	1	0.045			150	DO41
11-25268-04	400	1	0,045			150	DO41
11-25268-05	600	1	0.050			250	DO41
11-25268-06	800	1	0.060			500	DO41
11-25268-07	1000	1	0.060			500	DO41
11-12594-01	200	3	0.140			200	DO41
11-12594-02	600	3	0.140			200	DO41

Table 4-13: Switching Diodes, Axial Leaded (FCD BC)

Part Number	Voltage (V)	Current Rating	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-16475-00	75	500MW	0.0085	Flat	Philips	4 ns	DO35
11-09517-00	75	150mA	0.0090	Flat	Philips	4 ns	DO35

Table 4-14: Switching Diodes, Surface Mount (FCD BR)

Part Number	Voltage (V)	Configuration	Current Rating (mA)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-24837-01	70	Single	150	0.024	Down	Hewlett Packard	15	SOT23
11-24837-02	70	Common Cathode	150	0.04	Down	Hewlett Packard	15	SOT23
11-24837-03	70	Common Anode	150	0.04	Down	Hewlett Packard	15	SOT23
11-24837-04	70	Series	150	0.032	Down	Hewlett Packard	15	SOT23

Table 4-15: Transient Suppressors, Through-hole(FCD BE)

Part Number	Voltage (V)	Type	Power (W)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-23569-01	120		600	0.15	Flat	Motorola, GI	DO15
11-28275-01	10	Bipolar	600	0.25	Flat	Motorola, GI	DO15
11-26344-01	22	Bipolar	600	0.27	Flat	Motorola, GI	DO15
11-32715-01	10	Bipolar,5%	400	0.25	Flat	GI	DO41
11-32715-02	22	Bipolar,5%	400	0.25	Flat	GI	DO41

Table 4-16: Voltage Transient Suppressors, Surface Mount (FCD BE1)

Part Number	Voltage (V)	Type	Power	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-32571-01	26		600 W	0.27	Down	Motorola, GI	SMB
11-32571-02	6		600 W	0.27	Down	Motorola, GI	SMB
11-32571-03	5		600 W	0.25	Down	Motorola, GI	SMB
11-32571-04	12		600 W	0.25	Down	Motorola, GI	SMB
11-31725-01	8.5	Bipolar	600 W	0.37	Down	Motorola, GI	SMB
11-31725-03	18.8	Bipolar	600 W	0.37	Down	Motorola, GI	SMB
11-35427-01	33		1.5 kW	0.32	Down	Motorola, GI	SMC

Table 4-17: Diode Assemblies, Through-hole (FCD BF)

Part Number	Voltage (V)	Description	Current Rating (A)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-15369-00	50	1 Phase	1	0.16	Flat	GI	4PIN DIP
11-29879-01	600	1 Phase	6	0.84	Flat	GI	4PIN SIP

Table 4-18: Diode Arrays, Through-hole (FCD BG)

Part Number	Voltage (V)	Description	Current Rating	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-18548-00	50	8 Diodes	350 mA	1.00	Up	National Semiconductor	16 Pin DIP

Table 4-19: Diode Arrays, Surface Mount (FCD BG1)

Part Number	Voltage (V)	Description	Power Rating	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-35177-01	40		500 mW	1.00	Down	Motorola	14 Pin SOIC

Table 4-20: SCRs and TRIACs (FCD BH)

Part Number	Voltage (V)	Description	Current Rating (A)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-34127-01	600	SCR	16	0.45	Flat	Motorola	TO220
15-19536-01	50	TRIAC	8	0.36	Flat	Motorola	TO220

Table 4-21: PIN Diodes (FCD BI)

Part Number	Voltage (V)	Power Rating	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	Case
11-33224-01	100	250 MW	0.80	Down	Hewlett Packard	SOT 23

Table 4-22: Ultra-Fast Rectifiers, Through-hole (FCD BJ)

Part Number	Voltage (V)	Configuration	Current Rating (A)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-25375-01	50		1	0.055	Flat	Motorola, GI	35	DO41
11-25375-02	100		1	0.056	Flat	Motorola, GI	35	DO41
11-25375-03	150		1	0.10	Flat	Motorola, GI	35	DO41
11-25375-04	200		1	0.11	Flat	Motorola, GI	35	DO41
11-26662-02	100		3	0.15	Flat	GI	50	DO201
11-17555-00	150	Common Cathode	16	0.35	Flat	Motorola, GI	35	TO220
11-17555-01	200	Common Cathode	16	0.35	Flat	Motorola, GI	35	TO220

Table 4-23: Ultra-Fast Rectifiers, Surface Mount (FCD BJ1)

Part Number	Voltage (V)	Configuration	Current Rating (A)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-36653-01	100		1	0.45	Down	Motorola	35	SMB
11-36653-02	200		1	0.46	Down	Motorola	35	SMB
11-36654-01	100	Common Cathode	6	0.42	Down	Motorola	35	D PAK

Table 4-24: Schottky Diodes, Through-hole (FCD BM)

Part Number	Voltage (V)	Configuration	Current Rating (A)	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-22301-01	30		1	0.12	Flat	Motorola, GI	0	DO41
11-32381-01	40		3	0.17	Flat	Motorola, GI	0	DO15
11-22258-01	45	Common Cathode	30	0.75	Flat	Motorola, International Rectifier	0	TO220
11-31494-01	45	Common Cathode	80	4.70	Down	International Rectifier	0	D61

Table 4-25: Schottky Diodes, Surface Mount (FCD BM1)

Part Number	Voltage (V)	Configuration	Current Rating	FY93 Std. Cost ($)	Cost Trend	AVL Supplier(s)	trr (ns)	Case
11-28837-01	8	Dual-Series	200 MW	0.17	Down	Hewlett Packard, Siemens	0	SOT23
11-28837-03	30	Single	200 MW	0.15	Down	Hewlett Packard	0	SOT23
11-28837-04	70	Single	200 MW	0.15	Down	Hewlett Packard	0	SOT23
11-29267-01	8	Common Anode	200MW	0.22	Down	Hewlett Packard	0	SOT23
11-29267-02	8	Common Cathode	200 MW	0.22	Down	Hewlett Packard	0	SOT23
11-29267-03	8	Single	200 MW	0.20	Down	Hewlett Packard	0	SOT23
11-33298-02	40		1 Amp	0.30	Down	Motorola	0	SMB
11-33298-03	30		1 Amp	0.23	Down	Motorola	0	SMB
11-36028-01	20	Common Cathode	6 Amp	0.45	Down	Motorola	0	D PAK
11-36259-01	45	Common Cathode	15 Amp	0.75	Down	Motorola	0	D2 PAK

4.3.3 Diode Design Guide

Table 4-26 show the different technologies available and lists standard package types, power ratings, and other significant parameters. Detailed characteristics and major parameters for each family are discussed following the table.

Table 4-26: Diode Technology Comparison Matrix

FCD	Technology	Package	Voltage Range	Current/ Power Range	Reverse Recovery Time	Cost
BA	Zener Diodes	Leaded: DO35 DO41 DO15	1.8V - 200V 3.3V - 100V 3.3V - 200V	500 MW 1W 5W	N/A	
	Temperature Compensated Zeners	DO35	6.2V 5%			
BN	SMT Zener Diodes	SMT: SOT23	2.4V - 60V (5%,2%)	260MW		
BB	Rectifiers	Leaded: DO35 DO41 DO15 TO220 TO218	50V through 1200V	0.2 – 0.5A 0.6 – 1A 3A – 11A 8A – 30A 30A – 60A	1 uS to 10 uS	
BC	Switching Diode	Leaded: DO35	10V through 200V	10mA - 0.5A	10ns	
BR	SMT Switching Diode	SMT: SOT23		5mA - 0.2A		
BE	Voltage Transient Suppressor, Unipolar	Leaded: CASE7 CASE1	5V - 200V 6.8V - 400V	600W @ 1ms 1500W @ 1ms	Picoseconds	
BE1	Voltage Transient Suppressor, Unipolar	SMT: SMB SMC	6.8V - 400V 6.8V - 91V	600W @ 1ms 1500W @ 1ms		
BE	Voltage Transient Suppressor, Bipolar	Leaded: CASE7 CASE1	6.8V - 400V 7.5V - 400V	600W @ 1ms 1500W @ 1ms		
BE1	Voltage Transient Suppressor, Bipolar	SMT: SMB SMC	6.5V - 43V 6.8V - 62V	600W @ 1ms 1500W @ 1ms		

Diode Technology Comparison Matrix (Continued)

FCD	Technology	Package	Voltage Range	Current/ Power Range	Reverse Recovery Time	Cost
BF	Diode/Rectifier Assemblies (Multiple devices In a single package)	4 Pin DIP 4 Pin In Line Pkg 4 Pin, 1–2 inch Square Molded Case w/Metal Base	50V - 800V 50V - 1200V	1 A	N/A	
BG BG1	Small Signal Diode Arrays Small Signal Diode Arrays, SMT	14 Pin DIP 16 Pin DIP Surface Mount 5014-5016	 10V - 50V	To 400 mA/ 600 MW	5 ns to 10 ns	
BH	SCR TRIAC	TO 92 TO 220 TO 218 TO 92 TO 220	25V - 400V 25V - 600V 25V - 500V 25V - 600V	To 0.8 A 8 A – 25 A To 0.8 A 6 A – 20 A	N/A	
BI	PIN Diodes	Surface Mount SOT23	To 100V			
BJ BJ1	Ultra-Fast Rectifiers Ultra-Fast Rectifiers, SMT	DO 41 DO 15 TO 220 TO 218 SMB SMC TO 252(D^2Pak)	50V - 1000V 50V - 1000V 50V - 100V 50V - 600V 50V - 200V	1 A 1 A–3 A 6 A–16 A 16 A–30 A 1A 3 A – 6 A	25 - 75 ns 35 - 100 ns 35 - 100 ns 35 - 60 ns 35 ns	
BM	Schottky Diodes Schottky Diodes, SMT	DO 41 DO 15 TO 220 TO 218 SOT 23 SMB SMC TO 252(D^2Pak)	15V - 15V - 35V - 20V -	1 A 3 A 7.5 A – 30 A 30 A 3 A		

4.3.3.1 FCD BA, BN: Zener Diodes

Characteristics:

- The reverse voltage across zener diode (VZ) will remain constant within a range of current going through the zener (normally at 10% through 50% of Izm). The VZ of a temperature

compensated zener diode will remain relatively constant over a wide range of temperature (measured as VZ in % change/°C).

Parameters:

- VZ = nominal zener reverse breakdown voltage. It will be specified with a tolerance and a test current IZT (normally IZT is at 1/4 maximum power point) at thermal equilibrium (TE) or pulse test condition.
- PD = power dissipation. It is specified at a special lead or case temperature and is limited by maximum junction temperature, die size, package, and lead size. PD = TL-TA/ROL-A or PD = TC-TA/ROC-A, ignoring reverse leakage current losses.
  - — For surface mount parts, the temperature reference point is usually at the solder connection between lead and printer circuit board. **Caution:** Underwriters Laboratory (UL) mandates that the temperature at any point on a printed-wiring board (PWB) be limited to 105°C, so derating power dissipation of devices may be necessary.
- ZZT = zener impedance = VZ/IZ. It is measured by modulating the IZT by 10% @ 60Hz to 1kHz and measuring the peak to peak voltage this generates.
- ZZK = zener knee impedance. It is measured at IZK. IZK is low current test current in reverse direction (normally 250 mA) and is 10% modulated as in IZT above.
- IZM = maximum dc reverse current allowed through the zener = PD rating/VZ rating.
- IR = maximum reverse leakage current measured at some reverse voltage VR, less than VZ.
- VZ = maximum zener voltage regulation for VZ at 10% to 50% of IZM.

4.3.3.2 BB, BF - Rectifiers (FCD BF = Multiple FCD BB in One Package)

- VRRM = peak repetitive reverse voltage maximum. Do not exceed this voltage as device damage may occur.
- IO = average rectified forward current maximum. Usually specified at single phase, resistive load at specified ambient temperature.
- VF = forward voltage drop at specified forward current (IF) at junction temperature (TJ) = 25°C.
- IR = maximum reverse leakage current with reverse voltage (VR) (normally at VRRM) applied at specified temperature (TJ).
- IFSM = nonrepetitive peak surge current. Usually at 1 cycle of 60 Hz at rated load.

NOTE: These devices are available in duals in 3 pin packages such as TO220, and TO218, in center tapped configurations, common cathode, and common anode for space and cost savings.

4.3.3.3 FCD BC, BR, BG, BG1: Switching Diodes

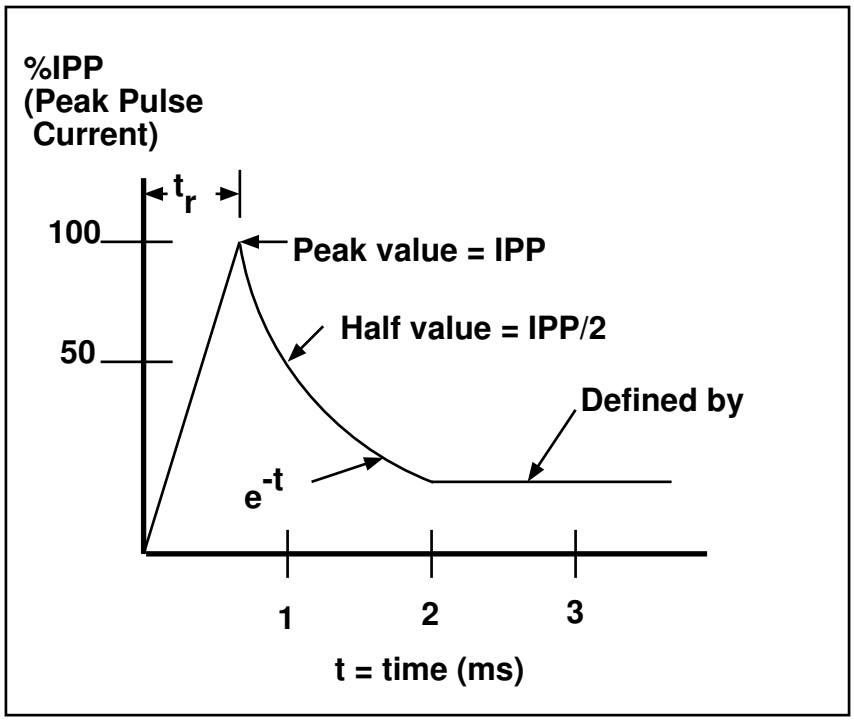
FCD codes BG and BG1 contain diode arrays —multiple FCD BC devices in one package. These devices are usually constructed of monolithic die with multiple junctions on a single die. This yields mostly matching parameters such as forward voltage drop, junction capacitances, switching times, and reverse breakdown voltages.

- VR = continuous reverse voltage maximum rating.
- V(BR) = reverse breakdown voltage. Measured at specified IBR = reverse test current (normally 100 mA).
- CD = diode capacitance. Measured at specified voltage VR at frequency = 1 MHz
- trr = reverse recovery time. Time required for diode/rectifier reverse current to go to zero when device is switched from forward conducting state to an applied reverse voltage (charge must be removed from junction before conductance stops).
- IO = average rectified forward current maximum. Usually specified at single phase, resistive load at specified ambient temperature.
- IFSM = nonrepetitive peak surge current. Usually at 1 cycle of 60 Hz at rated load.
- VF = forward voltage drop at specified forward current (IF) at junction temperature (TJ) = 25°C.

4.3.3.4 FCD BE, BE1: Voltage Transient Suppressors

- VRWM = working peak reverse voltage (nominal breakdown voltage).
- VBR = reverse breakdown voltage at test current IT.
- IR = reverse leakage current at rated VRWM.
- IRSM = maximum reverse surge current.
- Clamping voltage = VRSM (maximum reverse voltage at IRSM).
- Peak power dissipation (usually measured at 1 ms of exponential power pulse. See curve.)

Figure 4-2: Power Pulse Curve



4.3.3.5 FCD BH: SCRs and TRIACs

Characteristics:

The SCR consists of a main diode (usually a high current carrying diode) and a controlling gate that turns the main diode on or off. The main diode will have characteristics like the rectifier (FCD BB), but also parameters such as VRRM = peak repetitive blocking voltage (gate voltage = 0V, or negative voltage to ensure the main diode is off). This voltage has a critical rate of rise dv/dt which, if exceeded, may turn the main rectifier on when the gate signal is trying to keep the rectifier off.

A TRIAC is similar to an SCR except that it contains two main diodes connected back to back.

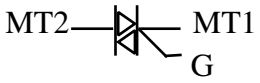
Parameters:

- IT(AV) is maximum average current that can flow through the main rectifier.
- ITSM is peak nonrepetitive surge current rating (usually one cycle, 60 Hz, preceded and followed by rated forward current and rated VRRM).
- PG(AV) = average gate power maximum.
- VFGM and VRGA = peak gate voltage, forward and reverse maximum.
- Peak forward or reverse blocking current = IDRM or IRRM = leakage current of main diode.
- VTM = on state voltage of main diode.
- IGT = gate trigger current maximum.
- VGT = gate trigger voltage.
- VGD = gate nontrigger voltage.
- IH = holding current (maximum current needed to flow through main diode to keep diode on).
- dv/dt = critical rate of voltage change across main diode. May cause false turn-on of main diode.

TRIACS: The TRIAC has all the parameters of the SCR with the following additional parameters:

- t on = turn-on time of main diodes relative to gate trigger signal.
- Gate trigger quadrants = gate voltage polarity relative to main terminal as shown in Figure 4-3.

Figure 4-3: TRIAC Gate Trigger Quadrants



Quadrant	MT2 polarity	MT1 polarity
1	+	+
2	+	-
3	-	-
4	-	+

4.3.3.6 FCD BI: PIN Diodes

The PIN diode is normally used as a high frequency signal switch. It is almost purely resistive at high frequencies, and the resistance can be varied from about 10K to less than 1 ohm by the control current (dc current in forward direction). Device selection would be to select reverse voltage rating, controlling current maximum, and on/off resistances.

4.3.3.7 FCD BJ, BJ1: Ultra-Fast Rectifiers

Includes all parameters of FCD BB (see subhead 4.3.3.2) plus:

- trr = reverse recovery time at specified IF = forward current.
- dif/dt = slope of current going through device from forward current (IF) to reverse current (IR) with respect to time (trr) measured in ns.
- Sometimes forward recovery time (tfr) is specified. It is the time a device takes for forward voltage (VF) to recover to some specified VF (usually 1V) when forward current switches from some forward current (IF) to zero at some specified dif/dt.

4.3.3.8 FCD BM, BM1: Schottky Diodes

Schottky diodes have all the parameters of standard rectifiers plus the following additional parameters:

- IRRM = peak repetitive reverse current. Power Schottky diodes have guard ring for stress protection. The guard ring reverse breakdown voltage is selected to break down approximately 10 V below the barrier breakdown.
- dv/dt = Critical rate of change of VR with respect to time. If exceeded, the diode may be damaged.
- ct = Capacitance normally tested at VR = 5 V, f = 1.0 MHz.

4.4 Resistors

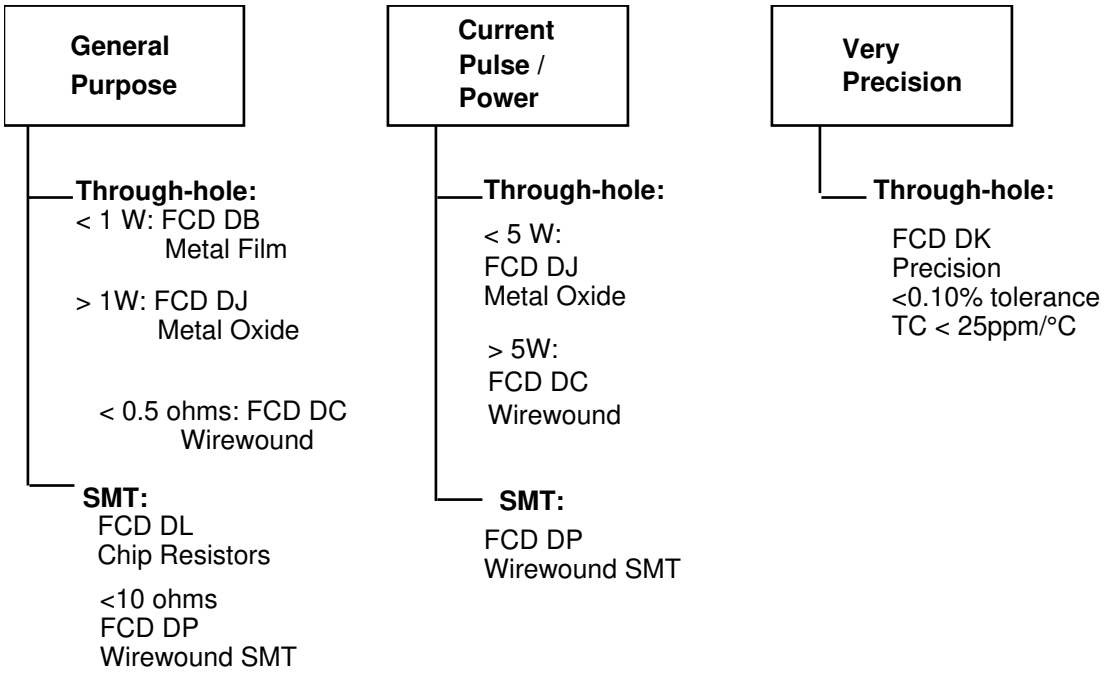
Fixed resistors are available in surface mount, axial and radial leaded, and chassis mount configurations. Resistance values range from below 0.01 ohms to 10 megohms and higher, with tolerances from 0.01% and tighter to 5%, and power dissipation capabilities from 0.100 watt and lower to 250 watts. Fixed resistors are subdivided into FCD codes by the base material used to produce the resistive element and by the package configuration. Table 4-27 lists these codes.

Table 4-27: Fixed Resistor FCD Codes

FCD	Description
DB	Metal Film
DC	Wirewound - Through-hole
DJ	Metal Oxide - Through-hole
DK	Very Precision - Through-hole
DL	Chip Types - Surface Mount
DM	Vertical Mount - Through-hole
DP	Wirewound - Surface Mount

4.4.1 Resistor Selection Guide

- Resistor technologies by application



4.4.1.1 Preferred Resistor Technologies

Certain technologies and configurations have been selected as Digital *preferred* products to maximize inventory, minimize part proliferation, and maximize total quantities to achieve the lowest piece price. General purpose devices such as metal film (DB), metal oxide (DJ) for through-hole, and chip resistors (DL) are the preferred technologies and are the most cost effective for high volume applications.

Preferred parts include most industry standard decade values (see Table 4-33) and should be used whenever possible. Additional values within the listed preferred technologies can be added if required by the application. The other technologies: wirewound, through-hole (DC), wirewound, surface mount (DP), very precision (DK), and vertical mount (DM) should only be used when there is a defined application need.

4.4.1.2 Surface Mount Resistor Technologies

Thick Film Chip Technology (FCD DL): These are supplied in industry standard sizes: 1210, 1206, 0805, 0603, and 0402 with 1210 rated at 1/2 watt, 1206 rated at 1/4 watt, 0805 rated at 1/10 watt, and both the 0603 and 0402 rated at 1/16 watt. The 0603 and the 0402 are not currently qualified for use in Digital.

The 1206 package is currently classified as *available*. Currently, 0805 is the preferred package. In the near future, the 0603 is likely to become the preferred package.

Higher wattage and larger sizes (greater than 1210) are not recommended for use because they can cause charring on the board surfaces. The standard tolerance to be used for all sizes is ±1%, with a maximum temperature coefficient of 100 part per million (ppm) change per °C. Tighter tolerances and temperature coefficients are not recommended. These devices are not recommended for use in current pulse applications.

Thin Film Chip Technology (also in FCD DL): Currently are qualified in the 1206 size; the 0805 size is not qualified nor recommended because of limited availability in the marketplace. The standard tolerance is ±0.1% with a maximum temperature coefficient of 25 ppm change per °C. Do not use for current pulse applications.

Wirewound Technology (FCD DP): Qualified in only three wattage sizes: 0.50, 0.70, and 1.2 watts. Higher wattages shall not be used. Both the 0.70 and 1.2 watt devices have been reduced from what the industry rates them to prevent charring on the board surfaces. The actual power dissipation should not exceed 0.25, 0.35, and 0.60 watts on these devices. Use shall be limited to applications that require values less than 3.0 ohms, actual power dissipation exceeds 0.125 watts, and pulse current applications. The standard industry tolerance is 3%, with 1% available.

4.4.1.3 Through-hole Resistor Technologies

Carbon Technology, FCD DA, shall ***not*** be used in Digital designs. Any use of this technology will require specific justification. It can be replaced with either metal film technology, DB FCD, for low power general purpose applications and either metal oxide, DJ FCD; or

wirewound, DC FCD, for high power general purpose and current pulse applications. Carbon film, DI FCD, is not recommended and should be replaced with metal film, ±1%, DB FCD, technology.

Metal Film (FCD DB): Devices are available for general purpose applications in 1/4, 1/2, and 3/4 watt sizes, with standard tolerances of 1.0% and 0.1%, and maximum temperature coefficients of 100 and 25 ppm change per °C. Other tolerances and temperature coefficients (ppm) shall not be specified. Nonstandard values shall be specified only in the 0.1% tolerances and 25 ppm devices. The 3/4 watt devices are not machine insertable and should only be used when a 1% tolerance is required; the preferred part would be a 1 watt metal oxide at 5% tolerance. These are not recommended for use in current pulse applications and the 0.1% tolerance devices shall not be used in these applications. Vertical mounting is not recommended.

Metal Oxide (FCD DJ): Recommended for high power applications where the actual power dissipation is in excess of 0.25 watts, and tolerance requirements are greater than 1.0%. Devices are available in 1, 2, 3, 5, and 10 watt power ratings. The standard Digital tolerance is 5%, with a tighter tolerance of 2% being available. Only the 1 watt devices are machine insertable, with the balance having to be hand inserted. The 1 and 2 watt devices, assuming that the actual power is 1/2 that of the rated power, can be mounted directly to the board surface. All other devices shall be mounted off the surface of the module through either special preforms or mounting techniques, for example, ceramic stand-off insulators installed on the leads and so forth.

Standard devices can be used for the majority of the current pulse applications; however, a thicker element is available for high current applications. Vertical mounting shall not be used.

Wirewound (FCD DC): Use is limited to very low ohm devices, less than approximately 0.3 ohms; very high power, in excess of 5.0 watt actual power dissipation; physical size restrictions, and very high current pulse applications. Devices are available in power ratings from below 1 watt to as high as 250 watts (higher wattages are restricted from use). **Note:** The power ratings on these devices are stated at +25°C and need to be derated as temperature increases. Devices are axial leaded to as high as 10 watts, after which two configurations are recommended: flat style for general purpose and aluminum housed for tighter space requirements.

Axial leaded, rated 2 watt and lower, can be mounted directly to the board surface; however, all others shall be mounted above the board surface using either a special preform or ceramic stand-off insulators installed on the leads. Devices dissipating power in excess of 5 watts are not recommended for module mounting; an exception is the vertical mount devices, FCD DM. The industry standard tolerance is 3.0%, with 1.0% available. Use of tighter tolerances is not recommended. Custom devices using long lead lengths for vertical mounting shall not be used.

Vertical Mount Power (FCD DM): Provides a means of mounting all high power technologies in a vertical mount position. Four different technologies are available in this configuration: metal film, metal oxide, wirewound, and wire. All of the rules previously presented for each of the individual technologies will apply here. Metal film shall be used only for tight tolerance designs, for example, 1%. Metal oxide shall be used in general purpose applications that require less stability and tolerance; the standard tolerance is 5%. Wirewound and wire shall only be used in applications that require low ohm values, high current pulses, and so forth. The standard tolerance is 5%, with 1% and 3% available.

Devices are available in 2, 3, 5, 7, 10, 15, and 20 watt power ratings. However, metal film devices are only available in 2, 3, and 5 watt ratings. The 2, 3, 5 watt devices require two hole mountings and the balance require multiple mounting holes. Extreme care shall be exercised when calculating the actual power dissipation that is allowed on the module surface. (Reference the General Specification typical temperature rise curves.) Both the 15 and 20 watt devices shall dissipate less than 50% power when mounted on a module.

Precision (FCD DK): Use is restricted to those applications where the industry standard 0.1% tolerance/25 ppm metal film resistor will not provide the stability and/or tolerance required. The industry offers three basic technologies: wirewound, metal film, and bulk metal to achieve the very tight tolerances and temperature coefficients. The preferred technology for use in all designs is bulk metal.

4.4.1.4 Selection Criteria and Guidelines

In order to select the right resistor for a given application, consider the following factors:

- Resistance value
- Resistance tolerance
- Effect of temperature change on the resistance value
- Worse case power dissipation
- Surface mount or through-hole packaging
- Resistor technology (application driven)
- Method of assembly

4.4.1.5 Steps In Selecting A Fixed Resistor

Use standard industry resistance values. Try to use the standard decade values listed in the Preferred Parts List. Industry standard values for each basic tolerance range are shown in Table 4-33. Nonstandard values are only available in certain technologies and their use will impact availability and cost.

Use industry and Digital standard tolerances within each technology. Try to standardize on 1% for general use. Do not under-specify a tolerance because in most cases this will only duplicate inventory in Digital without achieving any cost savings on the device. Similarly, do not over-specify beyond standard tolerance because it adds to the cost.

Select a technology/device which provides for twice the actual power to be dissipated at the maximum ambient temperature. There may be several choices available; however, the application requirements, assembly techniques, and physical size constraints will generally lead to the proper choice from the recommended/preferred table.

4.4.2 Resistor Preferred Parts

At this writing, there are too many preferred resistors to include a list in the Techfile. A table of preferred parts, and their characteristics, is available for online searching. This table is in the

form of a text file, and is located in the directory detailed in Table 4-28.

The recommended/preferred parts shown in the table are very complete, showing the basic resistance technology, significant design parameters, basic construction for assembly purposes, insertion or onsertion codes, cost per device and the General General Specification number where additional data can be obtained. Qualified suppliers can be obtained from the SPOC data base.

Table 4-28: Resistor Preferred Parts

- **Located at:**
  GOLF::DISK$TRACKREP:[3CB$SHARED.TECHFILE]fixed_resistors.txt

This file may be copied to your local directory, or searched remotely. Example 4-1 shows how to search the file to locate preferred parts.

Example 4-1: Searching the Preferred Part table

The file FIXED_RESISTORS.TXT is organized as shown below:

```
                    FIXED RESISTORS - RECOMMENDED/PREFERRED DEVICES   (* - PREFERRED USAGE)       REVISION LEVEL:  1

                                                                                                                DIGITAL
       USE   PWR      PWR    R TOL  PWR  MAX  ZERO  INS-                                                      PART
DCR@25C (*)  @25 C    @70 C  @25 C  TEMP DCWV MAX RTC  ONS-  CODE FCD  TECHNOLOGY/CONFIGURATION   GENERAL   NUMBER      COST
                                                          COMMENTS                                   SPEC
-------------------------------------------------------------------------------------------------------------------------------
 0.005       3.0             1.0    275        750       HB   DC   WW-AXIAL LEAD-MOLDED SILICONE U 1300004GS 133451701   0.205
 0.01    *   3.0             3.0    275        300       HB   DC   WW-AXIAL LEAD-MOLDED SILICONE U 1300004GS 131783500   0.20
 0.01        3.0             1.0    275        300       HB   DC   WW-AXIAL LEAD-MOLDED SILICONE U 1300004GS 132319101   0.205
 0.01    *   3.0             3.0    275        400       HB   DM              WW-VERTICAL MOUNT 1300015GS 133125201   0.44
 0.02    *   3.0             3.0    275        200       HB   DC   WW-AXIAL LEAD-MOLDED SILICONE U 1300004GS 131783400   0.20
 0.02        5.0             1.0    275        100       HB   DC   WW-AXIAL LEAD-MOLDED SILICONE U 1300004GS 132357201   (0.3985)
```

The parts flagged with an asterisk (*) are the preferred parts.

When using the VMS Search command, be sure to allow for spaces in values. For example:

SEARCH GOLF::DISK$TRACKREP:[3CB$SHARED.TECHFILE]fixed_resistors.txt "1.00K"

will not find any matches because there is a space between "1.00" and "K" in the file.
Note: This file will be updated as needed. If you create a local copy of this file, be sure to check for updates by using the DIRECTORY/DATE command on the master file on GOLF.

4.4.3 Resistor Design Guide

The comparison matrices on the following pages show the major characteristics, applications, and range of values available for each technology. Detailed characteristics and application guidelines for each resistor family are shown following the tables.

Table 4-29: Comparison Matrix: Axial-leaded Devices (FCD DB, DC, DJ, DK)

FCD	Package	Technology	Application	Max. Rated Power @25°C	Max. Rated Power @70°C	Value Range (ohms)	Max. Temp Coefficient (ppm/°C)	Tolerance (%)
DB	Axial Lead Through-hole	Metal Film	General Purpose		1/4	1.0 - 9.76 10.0 - 1.0 M 1 M - 22.1 M	100	1.0
			Precision		1/4	10 - 2.5 M	25	0.1
			General Purpose		1/2	1.0 - 9.76 10.0 - 1.0 M 1.1 M - 8.0 M	100	1.0
			Precision		1/2	10 - 2.5 M	25	0.1
			General Purpose		3/4	1.0 - 15 M	100	1.0
			Precision		3/4	10 - 2.5 M	25	0.1
DC	Axial Lead Through-hole	Wirewound	Low ohm/ current pulse	1.0		0.01 - 0.10 0.10 - 0.99 1.0 - 9.9 10 - 10.4K	400-125 90 50 20	3.0 1.0 Available
				3.0		0.01 - 0.20 0.21 - 0.99 1.0 - 9.9 10 - 15K	350-25 90 50 20	
				5.0		0.01 - 0.30 0.31 - 0.99 1.0 - 9.9 10 - 58.5K	200-25 90 50 20	
			General Purpose Current Pulse	10.0		0.1 - 0.99 1.0 - 9.9 10 - 167K	90 50 20	
DJ	Axial Lead Through-hole	Metal Oxide	General Purpose		1.0	0.20 - 9.1 10 - 68K 75K - 1.0M	350 350 200	5.0 5.0 2.0 Avail.
					2.0	0.22 - 9.1 10 - 100K 110K - 560K	350 350 200	5.0 5.0 2.0 Avail.
					3.0	0.22 - 9.1 1.0 - 100K	300 300	5.0 5.0 2.0 Avail.
DK	Axial Lead Through-hole	Bulk Metal	Very Precision		1/4 - 1/2	5.0 - 500K	1 - 4	0.01 - 0.1
					0.3 - 1.0	0.5 - 1.0M	2.5	0.005 - 1.0

Table 4-30: Comparison Matrix: SMT Devices (FCD DL, DP)

FCD	Package	Technology	Application	Max. Rated Power @25°C	Max. Rated Power @7°°C	Value Range (ohms)	Max. Temp Coefficient (ppm/°C)	Tolerance (%)
DL	Chip-SMT 0805 size	Thick/Thin Film	General Purpose		0.10	5.1 - 9.76 10.0 - 1.0M 1.1M - 5.0M	300 100 300	5.0 1.0 5.0
	1206 size				0.25	3.0 - 9.76 10.0 - 1.0M 1.1M - 22.0M	300 100 300	5.0 1.0 5.0
	1210 size				0.50	10.0 - 215K 221K - 1.5M	100 200	1.0
	1206 size		Precision		0.125	49.9 - 1.0M	25	0.1
DP	Surface Mount	Wirewound	Low ohm/ current pulse	0.5		0.10 - 0.99 1.0 - 9.9 10.0 - 1.41K	90 50 20	3.0 1.0 Avail.
				0.7		0.10 - 0.99 1.0 - 9.9 10.0 - 2.77K	90 50 20	
				1.2		0.10 - 0.99 1.0 - 9.9 10.0 - 10.4K	90 50 20	

Table 4-31: Comparison Matrix: Vertical Mount Resistors 2—5 Watt (FCD DM)

FCD	Package	Technology	Application	Max. Rated Power @25°C	Max. Rated Power @7°°C	Value Range (ohms)	Max. Temp Coefficient (ppm/°C)	Tolerance (%)
DM	Vertical Mount Through-hole	Low-ohm wire	General Purpose Current Pulse	2.0		0.01 - 0.049 0.05 - 0.10	400 100	3.0
		Low-cost wirewound				0.10 - 0.99 1.0 - 100.0	800 400	5.0
		Wirewound				0.10 - 0.99 1.0 - 9.9 10.0 - 40.0K	90 50 20	3.0 1.0 Avail.
		Metal Oxide/Film	General Purpose		2.0	100 - 13.0K	400	5.0
		Metal Film				10.0 - 150K	50	3.0 1.0 Avail.
		Low-ohm wire	General Purpose Current Pulse	3.0		0.01 - 0.049 0.05 - 0.10	400 100	3.0
		Low-cost wirewound				0.10 - 0.99 1.0 - 100.0	800 400	5.0
		Wirewound				0.10 - 0.99 1.0 - 9.9 10.0 - 5.00K	90 50 20	3.0 1.0 Avail.
		Metal Oxide/Film	General Purpose		3.0	100 - 22.0K	400	5.0
		Metal Film				10.0 - 150K	50	3.0 1.0 Avail.
		Low-ohm wire	General Purpose Current Pulse	5.0		0.01 - 0.049 0.05 - 0.10	400 100	3.0
		Low-cost wirewound				0.10 - 0.99 1.0 - 100.0	800 400	5.0
		Wirewound				0.10 - 0.99 1.0 - 9.9 10.0 - 5.00K	90 50 20	3.0 1.0 Avail.
		Metal Oxide/Film	General Purpose		5.0	100 - 27.0K	400	5.0
		Metal Film				10.0 - 150K	50	3.0 1.0 Avail.

Table 4-32: Comparison Matrix: Vertical Mount Resistors 7—20 Watt (FCD DM)

FCD	Package	Technology	Application	Max. Rated Power @25°C	Max. Rated Power @70°C	Value Range (ohms)	Max. Temp Coefficient (ppm/°C)	Tolerance (%)
DM	Vertical Mount Through-hole	Low-cost wirewound	General Purpose Current Pulse	7.0		0.50 - 0.99 1.09 - 1.4K	800 400	5.0
		Metal Oxide	General Purpose		7.0	200 - 56.0K	400	5.0
		Low-cost wirewound	General Purpose Current Pulse	10.0		1.0 - 2.00K	400	5.0
		Metal Oxide	General Purpose		10.0	200 - 75.0K	400	5.0
		Low-cost wirewound	General Purpose Current Pulse	15.0		General Purpose Current Pulse	400	5.0
		Metal Oxide	General Purpose		15.0		400	5.0
		Low-cost wirewound	General Purpose Current Pulse	20.0			400	5.0
		Metal Oxide	General Purpose		20.0		400	5.0

4.4.3.1 DB: Metal Film—Through-hole

The primary use of this technology is for *general purpose* applications. Devices are available in values ranging from 10 ohm to 10 megohms, with lower and higher values available for special applications, in tolerances of 1.0% and 0.10%, with rated power dissipations of 1/4W, 1/2W, and 3/4W. Standard industry values shall only be used/specified in the 1.0% tolerances. In the 0.1% tolerance devices standard industry values are preferred; however, special applications can use/specify nonstandard values. This technology offers excellent long term stability with life expectancies to far exceed 10 years. This technology shall not be used in applications where short term, high energy pulses are involved as early life failures will occur.

4.4.3.2 DC: Wirewound—Through-hole

The value, power dissipation, and application requirements all play a role in using this technology. The primary usage of this technology is for low resistance values, less than 0.50 ohm, high current pulse energy dissipation, and high power dissipation requirements. For general purpose usage, with actual power dissipation of less than 2.5 watts, metal oxide technology, DJ, is the preferred technology to use. Specific value selection is not critical; however, it is cost effective to specify the 3% tolerance industry standard values. The standard industry tolerance is 3%, with 1% being available for special applications. Applications with current pulses having fast rise times can be affected by the inductance of the windings of this technology. A special winding technique, Ayrton-Perry, is available to minimize this inductance.

4.4.3.3 DJ: Metal Oxide—Through-hole

The primary purpose of this technology is for general purpose usage at higher power dissipations. Devices are available in values of 0.20 ohms to 1.0 megohms; the value extremities are dependent on rated power. The standard tolerance is 5%, with 2% being available for special applications. Rated power dissipations of 1W, 2W, 3W, and 5W are available. These devices can be used in short term, low energy current pulses, that is, snubber applications. Nonstandard industry values are not available.

4.4.3.4 DK: Very Precision—Through-hole

This technology shall only be used when the application requires tolerance values of less than 0.10% and/or temperature coefficients less than 25 ppm per °C of temperature change. The preferred technology to be used is bulk metal. Specific values can be specified with tolerances as low as 0.001%, temperature coefficients of 1 ppm to 25 ppm, and power ratings from 0.25W to 2.0W. Wirewound and precision film technologies should not be used unless the application requires these specific technologies.

4.4.3.5 DL: Chip Type - Thick and Thin Film—Surface Mount

There are two different technologies specified within this family of components: thick film ink and thin film deposition system. The thick film is the general purpose product for use across all the different applications; however, neither technology shall be used in current pulse applications. The standard tolerance of the thick film devices is 1%, with a temperature coefficient of 100 ppm/°C. Thin film technology is for those applications that require precision values and/or tight resistance changes with temperature, that is, tolerances of 0.01% and 25 ppm/°C temperature coefficients. Digital has approved only three industry standard sizes for use: 0805, 1206, and 1210. The sizes represent the rated power dissipation of each of these devices: 0.100 W, 0.25 W, and 0.50 W, respectively. Thin film technology is only available in the 1206 size and is rated at 0.125 W. Thick film resistance values are generally available from 10.0 to 1.0 megohms, with lower and higher values available in certain sizes at 5% tolerances and higher temperature coefficients. Thin film resistance values are limited to a range to 49.9 to 1.0 megohms.

4.4.3.6 DM: Vertical Mount—Through-hole

This FCD assignment describes a packaging configuration rather than a specific technology. There are four technologies that can be obtained in this form of packaging: single wire, wirewound, metal oxide, and metal film. The resistance value ranges are dependent on the technology selected. In general, the standard tolerance is 5%, with 1% and 3% being available in some technologies for special applications. The rated power dissipations range from 2W through 20W. Proper power derating is very critical when using 5 watt and higher devices. This type of configuration offers maximum manufacturing assembly cost savings, as well as maximum X/Y space savings on the module.

4.4.3.7 DP: Wirewound—Surface Mount

The primary usage of this technology is for low resistance values, below 10 ohms, high current pulse applications, and higher power dissipations, that can not be obtained in the surface mount chip technology (DL). The value ranges are very dependent on the rated power dissipations, size, and range from 0.1 to 14.7 K ohm, and rated power dissipations of 1/2 W, 1 W, and 2 W. Because of the potential of board charring over life and the noncompliance with UL temperature restrictions of 105°C maximum on FR4 material, the 1 W device has been rated at only 0.7 watts and the 2 W devices rated 1.2 watts for Digital designs. The standard tolerance is 3%, with 1% available for special applications.

Table 4-33: Fixed Resistor Standard Values And Tolerances (*=preferred)

5.0% 3.0% 2.0%	1.0%	0.1%	5.0% 3.0% 2.0%	1.0%	0.1%	5.0% 3.0% 2.0%	1.0%	0.1%	5.0% 3.0% 2.0%	1.0%	0.1%
10.0*	10.0*	10.0*			18.4			32.8		56.2	56.2*
		10.1		18.7	18.7	33.0					56.9
	10.2	10.2*			18.9		33.2	33.2*		57.6	57.6*
		10.4		19.1	19.1			33.6			58.3
	10.5	10.5*			19.3		34.0	34.0*		59.0	59.0
		10.6		19.6	19.6*			34.4			59.7
	10.7	10.7*			19.8		34.8	34.8*	62.0*	60.4	60.4*
		10.9	20.0	20.0*	20.0*			35.2			61.2
11.0*	11.0*	11.0*			20.3		35.7*	35.7*		61.9*	61.9*
		11.1		20.5	20.5*	36.0*					
	11.3	11.3*			20.8			36.1			62.6
		11.4		21.0	21.0*		36.5	36.5*		63.4	63.4*
	11.5	11.5*			21.3			37.0			64.2
		11.7		21.5	21.5*		37.4	37.4*		64.9	64.9*
	11.8	11.8*			21.8			37.9	68.0*		65.7
12.0*		12.0	22.0*				38.3	38.3*		66.5	66.5*
	12.1*	12.1*		22.1*	22.1*			38.8			67.3
		12.3			22.3	39.0*	39.2*				
	12.4	12.4*		22.6	22.6*			39.2*		68.1*	68.2*
		12.6			22.9		40.2	39.7			69.0
	12.7	12.7*		23.2	23.2*			40.2*		69.8	69.8*
		12.9			23.4		41.2	40.7			70.6
13.0*	13.0*	13.0*		23.7	23.7*			41.2*		71.5	71.5*
		13.2	24.0*		24.0		42.2	41.7	75.0*		72.3
	13.3	13.3*		24.3*	24.3*			42.2*		73.2	73.2*
		13.5			24.6			42.7			74.1
	13.7	13.7*		24.9	24.9*	43.0*	43.2*			75.0*	75.0*
		13.8			25.2			43.2*			75.9
	14.0	14.0*		25.5	25.5*		44.2	43.7		76.8	76.8*
		14.2			25.8			44.2*			77.7
	14.3	14.3*		26.1	26.1*		45.3	44.8		78.7	78.7*
		14.5			26.4			45.3*	82.0*		79.6
	14.7	14.7*		26.7*	26.7*		46.4	45.9		80.6	80.6*
		14.9	27.0*					46.4*			81.6
15.0*	15.0*	15.0*			27.1	47.0*	47.5*	47.0			
		15.2		27.4	27.4*			47.5*		82.5*	82.5*
	15.4	15.4*			27.7		48.7	48.1			83.5
		15.6		28.0	28.0*			48.7*		84.5	84.5*
	15.8	15.8*			28.4		49.9	49.3			85.6
16.0*		16.0		28.7	28.7*			49.9*		86.6	86.6*
	16.2*	16.2*			29.1			50.5			87.6
		16.4		29.4	29.4*	51.0*	51.1*		91.0	88.7	88.7*
	16.5	16.5*			29.8			51.1*			89.8
		16.7	30.0*				52.3	51.7		90.9*	90.9*
	16.9	16.9*		30.1*	30.1*			52.3*			
		17.2			30.5		53.6	53.0			92.0
	17.4	17.4*		30.9	30.9*			53.6*		93.1	93.1*
		17.6			31.2		54.9	54.2			94.2
	17.8	17.8*		31.6	31.6*			54.9*		95.3	95.3*
18.0*		18.0			32.0			55.6			96.5
	18.2*	18.2*		32.4	32.4*	56.0*				97.6	97.6*
											98.8

4.5 Transistors

This section discusses the families of transistors listed in the following table.

Table 4-34: Types of Transistors and Associated FCD Codes

FCD code	Technology	Preferred Packages
FA	Transistor,switch,NPN ≤6 watts	TO92
FB	General purpose amps, NPN ≤6 watts	TO92
FC	Transistor,power,NPN >6 Watts	TO220, TO247[1]
FD	Transistor,switch,PNP ≤6 watts	TO92
FE	General purpose amps,PNP ≤6 watts	TO92
FF	Transistor,power,PNP >6 watts	TO220, TO247[1]
FG	Transistor,power MOSFET,DMOS N&P channels	TO92, TO220, TO247[1]
FH	Transistor,NPN (surface mount)	SOT23
FI	FET,N-channel,surface mount	SOT23
FJ	FET,N-channel	TO92
FK	FET,P-channel	TO92
FL	Transistor, PNP surface mount	SOT23
FM	FET,P-channel,surface mount	SOT23
FN	Transistor,array,NPN/PNP	DIP
FN1	Transistor,array,NPN/PNP,SMD	SOIC
FN2	Transistor,array,MOSFET,SMD	SOIC
FO	Transistor,isolated gate bipolar	TO220, TO247[1]

[1] Full isolated versions of the TO220 and TO247, presently referred to as the *Full Pack*, are also preferred packages.

4.5.1 Transistor Selection Guide

The initial selection information will help in identifying the proper device and locating the part number in SPOC; alternative component selector systems may also help in identification. First determine the following:

- The basic function and technology
- Leaded or surface mount style
- The estimated power dissipation of your application

Compare these three criteria to an existing component class and find the associated FCD code in Table 4-34. If a new function or description code does not exist, contact the Techfile author for more information. Lists of preferred parts begin with Table 4-35.

4.5.1.1 Preferred Packages

The preferred surface mount packages listed in order of increasing power dissipation are: SOT23, D-PAK, and D^2 PAK. The SOT23 is the most common and preferred if the limited wattage rating permits.

The preferred leaded packages are in a dynamic state. Presently, the preferred packages in order of increasing power dissipation are: TO92, TO220, TO247 and the newer full isolated versions of the TO220 and TO247. The full isolated parts are now available world wide and offer the advantage of mounting isolation without using mica or silicon pads. The reduced hardware and assembly time is a definite plus over the conventional TO220 and TO247. The thermal performance is equivalent to the latter packages with mica or silicon, but are not as good as the bare copper TO220, or TO247 mounted directly on a flat heat sink. The leaded D-PACK, which is capable of housing a larger die and dissipating a bit more power than the TO92 is now becoming available from several U.S. and Far East sources.

4.5.1.2 Guidelines for Searching Acceptable Parts

Since many transistor applications are unique, there may be more instances where no suitable preferred parts are found. If this is the case, the following guidelines will help narrow the search among the existing acceptable parts.

1. Find the proper FCD code in Table 4-34 for the device technology and power level, if listed.
2. From SPOC, find the Approved Vendors Listing (AVL) for that FCD and the Vendor Code. SPOC can now be searched by FCD and vendor or by vendor part number, if known.
3. If an acceptable equivalent part number is not located in SPOC, then a search of equivalent part numbers from preferred vendors will most likely lead to a solution. Although a new part number request form will be needed to bring this device type in-house, AVL suppliers are already qualified for entire families of parts and need no part qualification. For new technologies, AVL suppliers have procedures in place and are approved to supply self-qualification data.
4. Non-AVL suppliers are to be avoided unless other options do not exist and an AVL exception is approved by Purchasing.

4.5.1.3 Selecting a Small Signal, Low-Power Device

To select a small signal low-power device follow these steps:

A. For application < 250 MW:

1. Use surface mount SOT23 if at all possible.

2. If surface mount is not a possible option, use the TO92 package. TO90s are available lead formed in TO18 pin circle to make manual insertion easier.

3. Do not use metal cans TO18, TO72, TO5, or TO39. Use standard parts; stay away from electrical selections or specials.

B. For application >250 MW:

1. For leaded applications:

   (a) Use TO220, TO247, or fully isolated versions for leaded applications. Do not use the TO218 bare tab device. Do not use TO126 unless there is no other option.

   (b) In most cases use MOSFET instead of bipolar unless no option is available. Use Avalanche rated MOSFET as preferred over nonavalanche types.

   (c) Design to operate junction temperature at about 100°C maximum.

   (d) Do not torque TO220 or TO247 to heat sink with electric wrench. Use a square metal washer above the tab on the T0220. Follow manufacturer's mounting specifications.

   (e) Non-surface mount rated devices may not survive the surface mount time-temperature soldering profile. All non-IC DIP array types must be manually inserted, but are solder-wave process compatible.

2. For surface mount:

   (a) Use SOT223, D-PACK, or D^2 PACK. Do not use SOT89 package.

   (b) Favor MOSFET over bipolar devices.

   (c) Design to operate junction temperature about 100°C.

   (d) Power dissipation of most parts mounted on FR4 type glass boards is no higher than the free-air rating. Board to solder temperature must not exceed the 105°C UL board temperature rating.

4.5.2 Transistor Preferred Parts Tables

4.5.2.1 Surface Mount Transistors

Table 4-35: PNP Transistors, Surface Mount (FCD FL)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std Cost ($)
15-24062-01	MMBT3906	SOT23	40	40	200	250	0.03
15-24063-02	MMBT2907A	SOT23	60	60	600	200	0.04

Table 4-36: NPN Transistors, Surface Mount (FCD FH)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std. Cost ($)
15-24060-02	MMBT3904	SOT23	40	60	200	300	0.03
15-33047-01	MMBT2369	SOT23	15	40	500	sw	0.05
15-33353-01	PZT2222A	SOT223	40	75	600	300	0.46

Table 4-37: N-channel MOSFET, Surface Mount (FCD FI)

Part#	Industry type #	Package	VDSS (Volts)	RDS on (ohms)	FY93 Std. Cost ($)
15-28960-01	2N7002LT1	SOT23	60	7.5	0.09

4.5.2.2 Leaded Small Signal Transistors

Table 4-38: NPN Switching Transistors, < 6 Watts (FCD FA)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std. Cost ($)
15-09524-00	2N3904	TO92	40	60	200	300	0.03
15-20857-01	MPS2369	TO92	15	40	500	sw	0.07
15-29729-01	2N6516	TO92	300	300	500	40	1.18

Table 4-39: PNP Switching Transistors, < 6 Watts (FCD FD/FE)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std. Cost ($)
15-09525-00	2N3906	TO92	40	40	200	250	0.03
15-38879-01	MPSH69	TO92	15	15	50	2000	Not on file
15-26728-01	MPS2907A	TO92	60	60	600	200	0.09
15-29728-01	2N6519	TO92	300	300	600	40	0.38

4.5.2.3 Leaded Bipolar Power Transistors

Table 4-40: NPN Power Transistors, > 6 Watts (FCD FC)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std. Cost ($)
15-14508-01	TIP121 (Darlington)	TO220	80	80	5	4	0.21
15-19270-01	TIP31A	TO220	60	60	3	3	0.18
15-31172-01	TIP48	TO220	300	400	1	10	0.38
15-32122-02	MJF16206	TO247 (FP)	500	1200	10	3	2.80

Table 4-41: PNP Power Transistors, > 6 Watts (FCD FF)

Part#	Industry type #	Package	VCEO (Volts)	VCBO (Volts)	IC (mA)	fT (MHz)	FY93 Std. Cost ($)
15-14509-00	TIP125 (Darlington)	TO220	60	60	5	4	0.17
15-23664-01	TIP32C	TO220	100	100	3	3	0.18

4.5.2.4 Leaded Power MOSFETs

Table 4-42: Leaded Power MOSFETs —N-channel (FCD FG/FJ)

Part#	Industry type #	Package	VDSS (Volts)	RDS on (Ohms)	ID (Amps)	PD (Watts)	FY93 Std. Cost ($)
15-37564-01	IRFP460	TO247	500	0.27	20	250	Not on file
15-27849-01	IRF642	TO220	200	0.22	16	125	0.88
15-31493-01	IRFP450	TO247	500	0.40	14	180	2.20
15-34908-01	MTP50N06E	TO220	60	0.025	25	150	1.00
15-23358-01	IRF530	TO220	100	0.16	14	79	0.39
15-23160-01	IRFD210	HD1	200	1.5	0.6	1	0.26
15-39571-01	MTW8N60E	TO247	600	0.5	8	180	Not on file
15-39535-01	MTW16N40E	TO247	400	0.3	8	250	Not on file

Table 4-43: Leaded Power MOSFETs —P-channel (FCD FK)

Part#	Industry type #	Package	VDSS (Volts)	RDS on (Ohms)	ID (Amps)	PD (Watts)	FY93 Std. Cost ($)
15-24009-02	IRFD9120	HD1	100	0.6	1	1	0.46

4.5.3 Transistor Design Guide

This section provides a description of each transistor family by FCD code. It also gives detailed data on design parameters, cost, packaging, and reliability.

4.5.3.1 FA: Transistor Switch, NPN, < 6 Watts

This leaded family of parts is now preferred only in the plastic TO92 package. This limits the power dissipation to 625 MW at an ambient temperature of 25°C. Higher power option packages like the metal can TO5 and T039 are not recommended unless other package options are not acceptable. The plastic TO126 is in the same power range as the TO39, but availability and the number of vendors supporting this package are decreasing. Some applications now jump from the TO92 to the TO220 package for needed power increase. A newer package option is the leaded D-PACK available from Motorola and a few Far East vendors. This bipolar technology has not changed much over the last 10 years. The package variations, moving to surface mount, and vendors pruning their product line are the most significant issues. When option allows, the SOT23 SMD device is preferred.

4.5.3.2 FB: General Purpose Amps, NPN < 6 Watts

Same as FCD FA above.

4.5.3.3 FC: Transistor Power, NPN >6 Watts

This bipolar activity has slowed in the last 3 years as new designs switch to power MOSFET technologies. Unless you have a unique application, do not use this FCD. Use MOSFET FCD code FG instead. If you must have a bipolar device, then use it only in TO220, TO247, or equivalent *Full Isolated* plastic pack. Do not use the old style TO218 package because many vendors are replacing them with TO247. When selecting an old part from the data base, be sure to check with the vendor and component engineer to be sure the part will be available in the near future and that the price has not gone up considerably.

4.5.3.4 FD: Transistor Switch, PNP < 6 Watts

Same as FCD FA above.

4.5.3.5 FE: General Purpose Amp, PNP < 6 Watts

Same as FCD FA above.

4.5.3.6 FF: Transistor Power, PNP > 6 Watts

The general package and information for FCD code FC also applies for the PNP bipolar devices except that the move to MOSFET FCD code FG is not as clear cut because of the smaller number of P channel types and the price difference.

4.5.3.7 FH and FL : Transistor NPN and PNP Surface Mount

These FCDs describe the basic SOT23 SMT package for NPN/PNP devices. The SOT23 is the preferred SMT package for all transistor type devices. The basic wattage and other characteristics of this family are detailed in the general specification 15-00004-GS.

4.5.3.8 FI and FM: N-Channel and P-Channel FETs Surface Mount

These families refer to both junction and MOS-type FETs. The preferred packages are the same as for all other surface mount discrete packages. In order of increasing power dissipation and size they are: SOT23, SOT223, D-PACK, and D^2 PACK.

4.5.3.9 FJ and FK: N-Channel and P-Channel FETs

These two families should refer to junction FETs only, but some MOSFETs have also been included. The only preferred package for this leaded family of devices is the TO92.

4.5.3.10 FO: Insulated Gate Bipolar Transistor (IGBT)

This family of power products is an extension of the DMOS or HEXFET power MOS technology. Our major MOSFET vendors also supply several high voltage power IGBTs. The processing and function of this part is similar to a MOSFET except for the addition of another N or P layer between the normal MOSFET and the drain to substrate interface. This additional layer forms a basic NPN or PNP output structure with the same basic MOSFET input characteristics. The introduction of another N or P layer, depending on the type channel, allows for minority carrier current injection and conductivity modulation of an otherwise thick drain region. This lowers the conduction losses of high voltage types significantly but the usual problems of minority carrier storage effects on switching times become a problem. Radiation to reduce lifetimes has produced devices capable of switching in the order of 100 ns and appear usable to about 100 kHz. Major new usage is in some motor drives, monitor deflection circuits and power factor correction circuits. The preferred power packages are the TO220 and TO247 plus the full isolated versions of each.

4.5.3.11 FN: NPN/PNP Transistor Arrays; FN1: NPN/PNP Transistor Arrays, SMD; FN2: MOSFET Arrays, SMD

The above family of arrays should be used with some caution, because availability and cost have historically been at a premium for individual parts, especially if the array is not a monolithic device. Unless device matching is a concern, individual parts, especially the SOT23, are preferred over the SOIC equivalents. The leaded TO92 carries a manual insert cost of 15 cents each that can offset the DIP IC premium, but availability is still a concern.

4.5.3.12 Surface Mount Devices (General)

- Packaging
  - — FCD codes FH, FI, FL, and FM utilize the SOT23 surface mount package which is the preferred SMD package when die size, lead count and power dissipation limits are acceptable. The industry standard 2N number approximation is good except for power dis-

sipation limitations for the SOT23.

— CAUTION: Any new transistor considered must have the same emitter, base, and collector pinout configuration as standardized in 15-00004-GS. Do NOT USE any so-called R for reverse E-B pinout. E-B pinout options of the leaded TO92 transistors in the late 70's created havoc in manufacturing and cost Digital millions. We will not repeat this mistake with the SOT23.

- Technologies
  — Bipolar: The NPN/PNP bipolar transistor FCDs previously listed reflect most commonly used general purpose types. Other device types in the SOT23 package are also excellent options for surface mount applications. The preferred parts shown are meant to maximize usage of a few device types when applications permit. RF transistors also exhibit excellent performance in this pack due to strip-line mount and low package parasitics.
  — MOS: The die size limitation of the SOT23 limits MOSFETS to low voltage and moderately high RDS (on) in the order of about 60 V and 10 ohms respectively.
  — JFETS: Also available.
- Industry Package and Technology Trends
  — The SOT23 is a world wide standard and will be available at low cost for years to come. The low profile option TO236AB allows side 2 wave by smaller package to board clearance for use of adhesives. The higher profile version is fast becoming obsolete.
- Manufacturing Process Compatibility
  — SOT23 has been qualified and used successfully in both IR and vapor reflow as well as side 2 glue and wave soldering processes. The part is robust for temperatures below 270°C for about 20 seconds. (Refer to the time-temperature process profile described in 15-00004-GS.)
  — Process related failure modes in the SOT23: No problems exist within the temperature limits of the reflow profile. Excellent shock and vibration immunity exists. The most common failure mode is the E or B bond wire opening after wave or IR process.
  — SOT23: The onsert code is OA.
- Bulk Packaging / Tape Reel / Marking
  — SOT23: Production - Tape and reel 8mm; single collector tab oriented adjacent to and on the sprocket hole side. **Note:** Do not change the part orientation; keep it standard.
  — Marking SOT23: The bulk package or reel has all part and Purchase Order marking requirements. The device size limits marking to the vendor logo and symbol and a 3-4 alphanumeric code that is not the same as the vendor part number. In general, different vendors have the same code. The marking code can be on the device specification or or on the QVL following the vendor part number and preceded by a slash (preferred).

- Storage And Process Impact
  - — SOT23: Extended storage in a normal manufacturing environment is not a major concern. In high humidity environments, extended storage (beyond 3 months) may affect solderability, or lead to moisture penetration.
- Availability/Time Trend
  - — SOT23: Availability for most types is excellent out several years as SOT23s replace more TO92 leaded applications. Many sources exist world wide with only slight mechanical package dimension variations.
- Maturity and Cost Trend
  - — Cost is now in the mature area of the learning curve. There is some degree of downward pricing pressure for the *jelly bean* variety which is at par or below TO92 leaded for most types. New functions with cost savings may be available in near future.
- Cost Sensitive Parameters
  - — SOT23:
    - * Transition frequency (Ft especially above 500 MHz)
    - * High voltage C to E or drain to source versus low on losses VCE or VDS
    - * High voltage versus fast switching for bipolar
    - * Low storage time versus VCE conductive losses for bipolar
- Custom or Nonstandard Parts
  - — SOT23: Custom electrical selections must be avoided. Manufacturers do not want selections in this high volume product. Marking space limitation and cost are major negatives.
- Analysis of Alternatives
  - — Packages: SOT23: Major limits on device power handling and small die size will require use of a medium power SOT223 plastic surface mount package. Thermal details of the SOT223 are detailed in 15-00005-GS. Basically the SOT223 increases room temperature power dissipation at 25°C ambient, 105°C Tj from 160 MW to 666 MW.

4.5.3.13 Reliability Considerations

Reliability models and failure rate data for different part classes can be found in the DREAM notebook. For more information on DREAM, contact the chapter captain listed in subhead 4.1.1.

The following data shows the impact of different application conditions on device reliability.

- Deriving Failure Rates From Accelerated Testing
  - — Reliability and failure rates are determined by high temperature reverse bias (HTRB) life testing at the maximum rated temperature of the device. These temperatures are 150°C and 200°C for plastic and hermetic metal can packages respectively. The highest

voltage rated junction (collector—base for a transistor, drain—source for a MOSFET and drain or source—gate for a junction FET) is biased at 80% of the maximum rating to determine the failure rate (FR) or MTBF under these assumed worse case conditions.

- Operating Junction Temperature
  - — Junction Temperature (Tj) is the fundamental parameter and predictor of reliable operation for all the FCD codes. The operating or application junction temperature (Tj) is a function of the ambient temperature (Ta) and device temperature rise due to power dissipation. The operating or application Tj must be less than the rated maximum for any reasonable failure rate except for very low duty cycle applications. The recommended design limits are 100°C to 125°C maximum.
  - — Temperature acceleration factors for silicon PN junctions are predicted by the Arrhenius Model. Refer to the DREAM notebook for the Arrhenius equation and examples.
- Voltage and Current Stress
  - — Voltage and current stress are also major contributors to failure. Devices should not be operated above the absolute maximum rated voltage or current. Operation at 80% or less of each maximum rating is recommended.
- Maximum Device Ratings
  - — Vendor specified maximum values apply to individual parameter stress limits not to simultaneous limits.
  - — Simultaneous application of current and voltage is limited by either forward bias or reverse bias device capability.
  - — Forward bias operation limits are normally constrained by the maximum power dissipation, forward bias safe operating area (FBSOA), reverse bias safe operating area (RBSOA) and/or BVCEO or LVCEO. Safe operating curves, both forward bias (FBSOA) and reverse (RBSOA), are normally related to and limited by the maximum desired operating junction temperature or FBSOA curve, whichever dominates respective limits. The recommended operating current or voltage should be 80% or less of the absolute maximum limits specified, unless peak power levels are the limiting factor indicated by SOA curves.

4.6 Crystals and Oscillators

Crystal oscillators are available in both surface mount and leaded packages. They operate from a single supply voltage and provide an output waveform compatible with several logic family loads such as CMOS, ECL, and TTL.

4.6.1 Crystal Oscillator Selection Guide

Preferred parts, and their characteristics, are listed in the tables that follow. In order to select the right oscillator for a given application, the following factors need to be considered:

- What technology is required? What logic family will the oscillator drive? (Note: this choice is not necessarily restricted to standard output levels, for example, an ECL oscillator can drive CMOS if levels are shifted.)
- What type of package –surface mount or through-hole?
- What frequency is required? (Frequency is limited by choice of package and technology.)
- What tolerance is required? (Tolerance impacts cost; see tables.)
- Are there any special cost or reliability constraints?

With these factors in mind, refer to the following tables for comparison of available parameters. Refer to the design guide for information on how the selection criteria interact (for example, cost versus tolerance) and how to achieve an optimal design.

4.6.1.1 Steps in Selecting an Oscillator

A. Optimum path (For frequency between 1.025 MHz and 66.6667 MHz, tolerance=100 ppm, 40/60 % SYM, +5 volt supply, TTL/CMOS output.)

1. For surface mount, see Table 4-44, FCD=JC. The package type is plastic SMT. For leaded parts, see Table 4-45.
2. Select the exact frequency and part from the part numbers listed. Refer to GS and detailed specifications for more information as required.
3. If not found, find a higher frequency that is binary divisible to the exact frequency and use external divide in design if practical.

B. For very low frequencies (For time-of-day or dynamic refresh clocks in the 10 kHz to 600 kHz range.)

1. The preferred part/family for low power consumption, battery operated time clocking function is a tuning fork type crystal as used in digital watches. The highest volume and most cost effective frequency is 32.768 kHz.
2. For other frequencies, see Table 4-46, FCD=JB1. The package type is plastic DIP. The basic part number family is 18-18800-xx. **Note:** Do not use metal-can DIL options.
3. If the frequency is not found, a new part number variation will be required. This family specification is for tight tolerance (20 ppm) for time-of-day accuracy. If

this tolerance is not necessary and 50 or 100 ppm is suitable, a new part number and family specification is recommended as the cost savings can be 50%. This part family is also qualified for the above frequencies.

4. The tuning fork crystal has a parabolic temperature coefficient and is only guaranteed over a +10°C to +50°C ambient. Tolerance will degrade rapidly outside this temp range. Refer to subhead 4.6.3.9 for tuning fork characteristics and application information. Operation for dynamic refresh should not be a problem as temperature degradation would still be less than 200 ppm from 0°C–70°C.

C. For frequencies above 66.6667 MHz. (For the higher frequency range, a metal-can DIP is still necessary.)

1. For frequencies between 66.68 and about 80 MHz/TTL output:
See Table 4-47, FCD=JB; the package type is Metal DIL.

2. For ECL output and frequencies from about 65 MHz to 200 MHz:
See Table 4-48, FCD=JB2; the technology is Crystal; the package type is Metal DIL.

4.6.2 Crystal Oscillator Preferred Parts Tables

Almost all oscillators are considered custom because of the uniqueness of the frequency. Proliferation of custom parts should always be avoided or used only when necessary. Custom oscillator parts have a built in lead time of about 16 weeks. Chance sometimes lowers this time, but do not count on it. If an oscillator is necessary, the second best choice is to exhaust the possibility of using an existing preferred part or preferred alternative.

For moderate or low volume requirements of (less than 10K), it is often more cost effective to use an existing part and consider binary division of an existing higher frequency compatible part. This is certainly effective for very low frequency parts when the divide-by gate is a *jelly bean.* If board space is critical or volumes are high, a new part may be necessary.

The following tables list the preferred parts and their major characteristics. The table headings list the units used.

Table 4-44: FCD JC: Plastic Surface Mount Crystal Oscillators

Common Parameters								
VCC ±5% (V)	ICC maximum (mA)	Pkg. Figure	Ta (°C) range	Tol ohms	Symmetry (%)	Approx. Cost $	In/ Onsert Code	GS Spec.
5.00	35	4-7	0-70	100	40/60	1.71	OD	18-05509-GS

Part #	Frequency (Mhz)	Load Range	Tri-State Output
18-31724-01	15.2064	10-TTL	Yes
18-31724-02	20.0000	10-TTL	Yes
18-31724-06	4.9152	4-TTL/CMOS	Yes
18-31724-07	2.4576	4-TTL/CMOS	Yes
18-31724-08	7.3728	4-TTL/CMOS	Yes
18-31724-09	40.000	4-TTL	Yes
18-31724-10	37.50	4-TTL	Yes
18-31724-11	24.00	4TTL/CMOS	Yes
18-31724-13	12.288	4-TTL/CMOS	Yes
18-31724-14	27.00	4/TTL-CMOS	Yes
18-31724-15	66.3552	CMOS	Yes
18-31724-16	36.00	CMOS	Yes
18-31724-17	66.00	CMOS	Yes
18-31724-18	66.6667	CMOS	Yes
18-31724-21	64.00	CMOS	Yes
18-31724-23	11.0592	4-TTL/CMOS	Yes
18-31724-25	31.3344	4-TTL/CMOS	Yes
18-31724-26	33.00	4-TTL/CMOS	Yes
18-30968-02	30.00	10/TTL	Yes
18-30968-05	20.00	10/TTL	Yes
18-30968-06	34.00	10/TTL	Yes
18-30968-07	10.00	10/TTL	Yes
18-30968-09	50.00	CMOS	Yes
18-30968-10	50.00	10/TTL	Yes
18-30968-11	25.00	10/TTL	Yes
18-30968-12	3.6864	1-/TTL	Yes

Table 4-45: FCDs JB/JB1: Plastic 14 pin DIP TTL and CMOS Crystal Oscillators

Part #	Freq. (MHz)	Vcc (±5 %)	Icc max (mA)	Pkg fig.	Ta range (°C)	Toler-ance (ppm)	Sym-metry	Load Range	Tr/T f (ns)	Tri-Sta ?	ENA /DIS ?	Comp Outs ?	App. Cost ($)	In/ Onsert Code	GS spec
18-35972-01	25.1748	5.0	35	8	0-70	100	40/60	10TTL	7	No		N	1.50	7	None
18-35972-02	64.0000	5.0	35	8	0-70	100	40/60	CMOS/ 50pf	7	No		N	1.50	7	None
18-35972-03	61.5385	5.0	35	8	0-70	100	40/60	CMOS/ 50pf	7	No		N	1.50	7	None

Table 4-46: FCD JB1: Plastic 16 pin DIP, Low-Frequency CMOS

Part #	Freq. (kHz)	Vcc (±5 %)	Icc max (uA)	Pkg fig.	Ta range (°C)	Toler-ance (ppm)	Sym-metry	Load Range	Tr/T f (us)	Tri-Sta ?	ENA /DIS ?	Comp Outs ?	App. Cost ($)	In/ onsert code	GS spec
18-18800-02	32.768	3.0-5.25	125	TBD	10-50	30	40/60	CMOS	1	No	No	No	3.50	8	None
18-18800-03	25.600	3.0-5.25	125	TBD	10-50	30	40/60	CMOS	1	No	No	No	3.50	8	None

Table 4-47: FCD JB: Hi-Frequency Metal DIL Crystal Oscillators

Part #	Freq. (MHz)	Vcc (±5 %)	Icc max (mA)	Pkg fig.	Ta range (°C)	Toler-ance (ppm)	Sym-metry	Load Range	Tr/T f (ns)	Tri-Sta ?	ENA /DIS ?	Comp Outs ?	App. Cost ($)	In/ onsert code	GS spec
18-11660-61	69.1968	5.0	60	4-9	0-70	100	40/60	10TTL	5	No		No	5.50	HJ	18-05507-GS
18-11660-88	83.0360	5.0	110	4-9	0-70	100	40/60	10TTL	5	No		No	5.50	HJ	18-05507-GS
18-11660-90	76.9000	5.0	110	4-9	0-70	100	40/60	10TTL	5	No		No	5.50	HJ	18-05507-GS
18-11660-91	74.3697	5.0	110	4-9	0-70	100	40/60	10TTL	5	No		No	5.50	HJ	18-05507-GS

Table 4-48: FCD JB2: ECL Crystal Oscillators @5V (non-tristateable)

Part #	Freq. (MHz)	Vcc ±5% (V)	Icc max (mA)	Ta range (°C)	Toler-ance (ppm)	Sym-metry	Load Range	Tr/Tf (ns)	ENA/ DIS ?	Comp Outs ?	App. Cost ($)	In/ onsert code
18-30295-02	80.2900	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	6.00	HJ
18-30295-03	160.00	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	10.00	HJ
18-30295-04	69.1968	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	6.00	HJ
18-30295-05	119.843	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	6.00	HJ
18-30295-06	143.000	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	10.00	HJ
18-30295-07	130.808	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	8.00	HJ
18-30295-08	114.285	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	7.00	HJ
18-30295-09	100.000	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	7.00	HJ
18-30295-10	93.800	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	7.00	HJ
18-30295-11	74.3697	5.0	110	0-70	500	40/60	ECL	2.5	No	Yes	7.00	HJ

Table 4-49: FCD JB2: ECLPS Complementary Output Crystal Oscillators for +5V

Common Parameters							
VCC ±5% (V)	ICC max (mA)	Ta (°C) range	Tol (ppm)	Symmetry (%)	App Cost $	In/ Onsert Code	Enable/ Disable
5.00	125	0-70	200	45/55	35.00	HJ	Y

Part #	Frequency (MHz)	Load Range
18-36376-01	300.00	ECLPS
18-36376-02	266.67	ECLPS

4.6.3 Crystal Oscillator Design Guide

Table 4-50: Comparison Matrix

FCD	TECH.	CRYSTAL TECHNOLOGY	PACKAGE	FREQUENCY (MHZ)	TOLER-ANCE (PPM)	COST
JC	CMOS/ TTL	AT Strip	Plastic SMT	1.025- 66.6667	Std: <100 Opt: < 50	2.20 add 25%
JB/ JB1	TTL/ CMOS	AT Strip AT disk	Plastic DIP (through-hole) Metal DIL (thru-hole)	1.025-66.6667 66.668-125	Std: <100 Opt: < 50 Std: <100 Opt: < 50 Opt: < 25	1.50 add 25% 5.00-45.00 add 20% add 80%
JB1	CMOS	Tuning fork	Plastic DIP	10-600kHz	Std: <100 Opt: < 50 Opt: < 25	 add 10% add 25%
JB2	ECL ECLPS	AT disk SAW	Metal DIL (thru-hole) Metal DIL (thru-hole)	65-200 200-800	Std: <200 Opt: <100 Std: <400 Opt: <200	8.00-200.00 45.00-85.00 add 10%

4.6.3.1 JB: Crystal Oscillators, TTL

This category originated from the old 7400 and 74LS series of TTL logic families. It presently covers the frequency range from 1 MHz to 84 MHz. Below 1 MHz, CMOS types are more effective; above 84 MHz, ECL or high speed CMOS devices are used. The primary package is the metal can dual in-line (DIL). Plastic DIPs are now available and preferred in the frequency range of 1.025 MHz to 66.6667 MHz. The plastic DIP uses a smaller AT strip crystal with better shock resistance and reliability. Auto insertion during assembly saves approximately another 20 cents over the manually inserted metal-DIL package.

4.6.3.2 JB1: Crystal Oscillators, CMOS

Originally this category was for low frequency CMOS types for low power consumption, but now it includes high speed CMOS to about 140 MHz. The primary package is the metal can DIL. Plastic DIPs are the preferred option in the frequency range of 1.025 MHz up to 66.6667 MHz.

4.6.3.3 JB2: Crystal Oscillators, ECL

Originally this category was for -5.2V operation with Motorola 10K and 10KH ECL families.

It now includes 100K and Motorola ECLPS output compatibility. The primary package is still the metal can DIL, with no plastic DIP or viable surface mount style in sight. Most ECL oscillators used within Digital are operated in pseudo- ECL mode to drive high speed Digital CMOS microprocessors and operate at +5V supply. This alternate power common technique requires a different pinout of the oscillator to keep the can at ground potential.

4.6.3.4 JC: Crystal Oscillators, Surface Mount

The AT strip crystal cut has made possible a family of plastic molded TTL/CMOS compatible parts in the frequency range of 1.025 MHz to 66.6667 MHz. The design of this family of parts is the same as the plastic DIPs in the TTL FCD code JB. The smaller crystal and automated mass production techniques for these parts have shown a substantial improvement in quality and reliability over the metal can DIL equivalents in the FY91/92 usage period in Digital manufacturing.

4.6.3.5 Major Parameter Definitions for all Oscillators

a. **Frequency Tolerance:** Specified in ppm. The standard for quartz crystal oscillators is 100 ppm or 0.01% overall tolerance. The overall tolerance is all inclusive and is the sum of i)initial calibration tolerance, ii)frequency changes over the operating temperature range, iii)frequency voltage coefficient over the Supply Voltage Range, iv)load range and v)aging. The 100 ppm limit is well within the nominal for quartz crystals. Relaxing to 200 ppm or 400 ppm is not cost sensitive except for ECL technology devices in the > 100 MHz range, where 500 ppm accuracy may be worth considering for very high volumes (>100K). Surface Acoustical Wave (SAW) resonators, used most effectively in frequencies above 250 MHz, have a nominal overall tolerance of 200 ppm. Relaxing to 400 ppm may have a reasonable price benefit if volume is in the 20K range.

b. **Supply Voltage Range:** The standard is normally 5.0 volts ±5%. Suppliers guarantee the stability or change in oscillator frequency over this supply range. Newer plastic DIPs and SMD parts have a wider guarantee of ±10% which is the standard for this series at no extra cost.

c. **Ambient Temperature:** The operating temperature range over which the part is guaranteed to be within the frequency tolerance ppm limit specified. The industry standard is 0°C to +70°C.

d. **Start-up Time:** Time for oscillator to be at proper frequency when supply voltage is at 5.0 V. It is normally 25 ms, with 10 or 15 ms available for some families. Designing for 25 ms is recommended. Very low frequency parts, such as time of day calendar oscillators operating in the 25–100 kHz range, use a tuning fork type crystal which has a very long start up time approaching seconds. Refer to the appropriate specification.

e. **Frequency Aging:** Change in crystal frequency due to aging characteristics of crystal attachments and surface properties. The industry nominal is 5 ppm per year. The change can be ± and usually occurs in the first 30 days. Subsequent aging of well designed crystals is in the ±1 ppm range after the initial early aging.

f. **Output Symmetry:** The high to low voltage time in the clock frequency period or duty

cycle of the output. The industry standard symmetry is 40% to 60% duty cycle. A tighter symmetry of 45/55% is available in some families as a special. The cost for tighter symmetry can be significant at high frequencies when the semi-amplifier propagation or phase delay is significant with respect to the clock period.

g. **Load Range:** Conforms to the logic family output drive capability. The older 10 TTL load compatibility for the 7400 series is outdated. Newer oscillator output drives are designed to drive 4 TTL or 50 pf CMOS type loads. This load option should always be selected when adequate. The only exception would be if an older preferred part exists and is specified for 10 TTL loading.

h. Tri-state/ Output Enable/Disable: Newer designs all incorporate this tri-stating function which enhances testability by disabling the oscillator in a high impedance state for board testing. Test signals can then be applied directly to the oscillator output with no damage to the oscillator. This function is now free in the 1.025 MHz to 66.6667 MHz frequency range for both the plastic DIP and plastic surface mount families.

Note: If a tri-state type oscillator is used with pin #1 open, the oscillator is enabled and functions exactly like the older part which had no connection to the E/D pin #1. The tri-state function should always be selected for new frequencies in the plastic DIP and SMD families ranging from >1.025 MHz to 66.667 MHz. For other families, tri-stating is not necessarily cost effective and should be implemented by external gating on the circuit board. The only other exception is the very high frequency SAW devices above 250 MHz which have an enable/disable function gate as used in ECL devices.

4.6.3.6 Crystal and Crystal Oscillator Characteristics

General description: The 18 class crystal oscillators are self-contained crystal controlled oscillators. They contain a quartz crystal, discreet or IC amplifier and, usually, additional phase correction RLC components. The output buffer is normally a conventional IC for ECL and TTL compatibility. All the circuit requires for oscillation is a loop gain >1 and 360 phase shift at the desired frequency only.

The construction of metal DIL packaged oscillators is a conventional thick film on alumina (ceramic) substrate, normally with thick film resistors and a combination of SMDs and/or wire bonded semiconductors. There are some variations to this process depending on the supplier and frequency of the part. The critical process is the mounting of the thin quartz disk about 1/4 inch in diameter and 0.010 inch thick suspended above the substrate by three small metal posts. This crystal is then adjusted to frequency by metal deposition or other mass variation process that makes the crystal oscillator unique from other types of hybrid circuits.

The construction of the plastic SMD and DIP devices is much simpler. The crystal is a smaller rectangular AT strip prepackaged in a miniature shell similar to digital watches. The IC is designed to have both the gain and phase required for oscillation. The crystal and IC are then bonded to a conventional metal lead frame and molded like SMD and DIP ICs. The crystal technology presently limits frequencies to below 66.6667 MHz.

4.6.3.7 Reliability Considerations

- Effect of Oscillators on System Reliability

The overall quality and reliability levels of the industry have improved significantly the last 10 years. However, the need for higher frequencies and the increase in population per board and system have far outstripped the perceived gain. It is not unusual to see small systems like Digital DECstations and workstations with 10 or 20 crystal or crystal oscillator clocks in a system configuration. The cost of failures must still be a significant percentage of material acquisition costs. The six sigma goal is still distant with the exception of a few lower frequency families. Quality and reliability must be improved 10–100 fold in the next few years even as frequencies and complexity increase. We must avoid repeat problems and control our end of potential process-induced problems as well.

- Parts per Million (ppm) Through Process

The best estimate of overall ppm levels through our manufacturing process is:

Metal DILs : 5000 ppm
Plastic SMDs : 100-500 ppm
Field failure information: Unknown to author

- Shock/Vibration

Quartz crystals have a real sensitivity to mechanical shock damage. For the most commonly used crystal cut, the AT cut, the thickness of the crystal is inversely proportional to the fundamental frequency of vibration. Blank thickness of a few mils results in a fragile mounting environment for the crystal which in many cases is the weakest link in the reliability chain. Because the AT cut vibrates in a thickness mode, the crystal must be suspended on metal posts. Dropping or mishandling of crystals may lead to complete breakage of the quartz or mount, or possibly cracking damage which will affect performance and service life. For example, dropping 18–22 MHz fundamental metal DIL oscillators a distance of about 30 inches could damage about 5% of the parts. The AT strip used in the plastic DIPs and SMDs have a smaller mass and mounting and thus a significantly better shock capability.

- Hermeticity

Because the quartz crystal mechanically vibrates at resonance, any mass changes on the surface will cause a change in frequency, an increase in its resistance and lowering of Q. These effects can cause an operating failure over time. The metal DILs are welded and hermetic, though no weld yield is six sigma. The Plastic DIPs and SMD parts contain the crystal in a cylindrical hermetic package with an overmolded plastic, in effect, a double seal. Solder sealed devices offer a reasonable seal but must not be used due to process compatibility problems.

4.6.3.8 Manufacturing Process Sensitivities

- Wave Solder Processes

Solder sealed parts are not to be used when subjected to the Digital wave-solder process. Solder seal breakage and leaks have caused a very high and unpredictable failure rate in the past. Metal DIL oscillators containing internal SN60/40 solder, or equivalent low melt temperature, have historically experienced solder dewetting problems in some facilities. The apparent inter-

nal solder melt temperature margin is insufficient and difficult to predict and control.

- New Vibrating Wave Process

The metal DIL has recently experienced solder wick shorting from the metal lead to package ground. NEL gold lead parts wick faster and have a smaller nominal glass standoff which aggravates the situation. Smaller PWB holes create hand insertion clearance problems and is not a good solution. Increased standoff heights are under consideration. Spacers are a short term solution. Lead trimming for length prior to board insertion must be done without stressing the lead to glass seal. If proper fixturing is not available, most metal DIL oscillator suppliers will trim length for a fee.

- SMT Processes

The plastic SMD parts have been qualified for both IR and vapor-phase reflow soldering. Refer to the appropriate specification for limits. The plastic DIP has the identical design and process as the SMDs except for the internal crystal package which uses a lower temperature. These devices can be auto-inserted and wave soldered but **must not** be subjected to the higher time temperature exposures of an SMD process.

- Insertion

Metal DIL packages must be hand inserted and then wave soldered. Hand insertion is costly and slow and the increased handling can lead to breakage of the crystal or glass metal seal. The plastic DIP eliminates all these problems in addition to the solder wicking problem.

- ESD

The CMOS oscillators are somewhat ESD sensitive, although the only function pins available to the outside world are the +5V, ground and the output. These are quite robust. ESD damage from handling has not been a problem.

- Bulk Packages

The metal DILs are shipped in IC sticks (tubes). They are not auto-insertable.
The plastic DIPs are also shipped in sticks, but can be auto-inserted.
The plastic SMDs are shipped taped and reeled on 24 mm tape.

4.6.3.9 Oscillator Characteristics and Performance Features

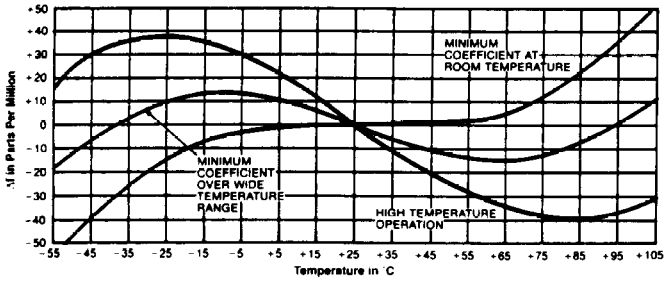
- Most Common Crystal Cuts and Technology—AT Cut

AT cut: Used in most Digital oscillators in both disk and strip form factors because of good temperature tolerance characteristics. Vibration is in a thickness shear mode. The present fundamental frequency range is approximately 4 MHz to 26 MHz. Below 4 MHz, the blank gets very thick (high resistance) and oscillator binary division is used to obtain lower frequencies. At higher frequencies, the blank gets too thin and fragile. The thickness of the blank is related to the fundamental vibrating frequency as: t=1660/f (with f in kHz, t in mm). For a fundamental frequency of 26 MHz, t=0.0638 mm or 0.0025 inch. Very thin and fragile to mount without cracking, especially in large disk form.

Temperature characteristics: The AT crystal cut exhibits a cubic frequency/temperature charac-

teristic with an inflection point at about 25°C. The temperature performance is controlled by accuracy of the crystal cut axis, as shown in Figure 4-5.

Figure 4-4: AT Crystal Cut Frequency/Temperature Characteristics


MINIMUM COEFFICIENT AT ROOM TEMPERATURE
MINIMUM COEFFICIENT OVER WIDE TEMPERATURE RANGE
HIGH TEMPERATURE OPERATION
Δf in Parts Per Million
Temperature in °C

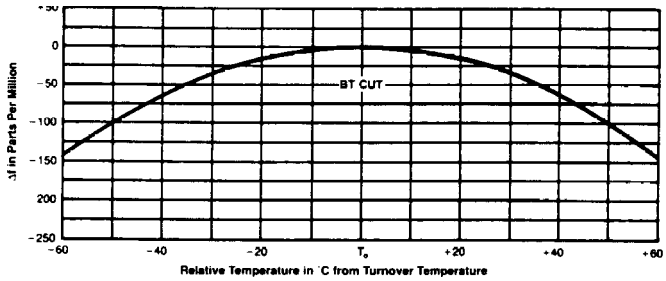
Vibrating overtones: The thickness shear mode in the AT cut can also be excited at odd value harmonics of the fundamental, that is, x3, x5, x7, x9 and so forth. The 9th and 11th overtones start getting low in energy resulting in circuit design complexity. In the AT family, a 40 MHz device would be designed using third OT crystal with its fundamental at 13.33 MHz. The oscillator design must now suppress the fundamental (13.33 MHz), the 5th OT(66.66 MHz) and possibly the ninth OT (120 MHz) unless the amplifier gain-bandwidth provides adequate reduction of the higher frequencies, which is usually the case.

Frequency limits: The AT cut has practical cost and reliability limits due to thickness and high order OTs of about 200 MHz which is a 22 MHz at the ninth OT. This limitation has led to new crystal technologies.

- BT cut

The BT cut crystal axis is also a thickness shear mode crystal with a thicker blank at high frequencies. This extends the upper frequency capability but results in poorer temperature-frequency stability. The BT cut frequency-temperature characteristic is parabolic. See Figure 4-6. Use of the BT cut in high frequency applications normally requires tolerance relaxation from 100 ppm to about 200 ppm or a reduction in the temperature range.

Figure 4-5: BT Crystal Cut Frequency/Temperature Characteristics



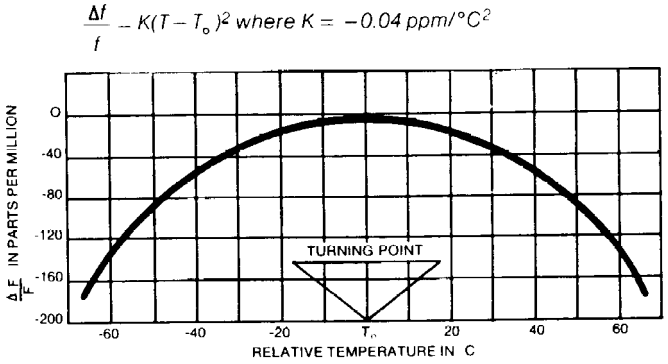
- Low Frequency: Tuning Fork

Nominal frequency in the 10–350 kHz range. Relatively low power drive capability but excellent for low power consumption applications, such as digital watches and clocks. Like the BT cut, the temperature-frequency characteristic curve is parabolic and limits the temperature stability to about 200 ppm over a 0°C–70°C range or about 30 ppm over a 40°C span centered at the turn-over temperature. See Figure 4-7.

Change in frequency in ppm is: df/f(ppm) = K(T-To)**2

Where T= temperature, To= turn-over temperature, and K=.04 ppm/C**2

Figure 4-6: Crystal Turning Point



- Symmetry

The industry standard output symmetry (duty cycle) is 40%/60%. Special selections in some frequency and technologies are cost effective and offered as options at 45%/55%. Selections of 45%/55% or tighter are available but can get expensive. The no cost 45%/55% option is available by suppliers in the low frequency ranges (less than about 30 MHz, depending on the manufacturer). For frequencies less than 12 MHz, the supplier process is normally to use a fundamental crystal with an internal edge triggered binary division. This essentially outputs a square wave. This technique can also be applied external to an oscillator by design.

At higher frequencies, the internal IC prop delay and tr/tf times degrade symmetry to near the 40/60 specification limit. Both degrade with temperature so this sensitivity is another concern over the 0°C–70°C range. The ECL compatible type is temperature compensated with controlled tr/tf and prop delay limits, so is a much better IC for high frequency. Tight 45%/55% symmetry is available in the 200-400 MHz SAW types.

Tight symmetry by division is realistic up to a maximum frequency depending on the manufacturer and technology. The problem at high frequencies is a thinner AT crystal, or using overtones (See subhead 4.6.3.9.) Overtones are fine, but now the circuit complexity increases as the lower odd harmonics have to be suppressed, and a lower level desired frequency has to be amplified. High frequency non-ECL symmetry improvement has a price, especially in the third or higher overtone range (>60 MHz). For frequencies less than 66.6667/2, it makes more sense to use a plastic SMT or plastic DIP with an external divider in all but the most critical space lim-

ited applications. At higher frequencies, suppliers normally use overtone devices and divide by 2 for symmetry improvement. However, the cost of crystal oscillators rises steeply and the trade-offs should be looked at and reviewed with the component engineer.

- Power Supply Ramp

In addition to normal bypass filtering, the power supply should rise with no major discontinuities and have a rise time of between 400 usec and 400 ms to guarantee the oscillator starts properly at the desired frequency and not at an undertone or overtone frequency.

- Power Supply Voltage By-Pass Capacitor

Digital design standards require specific bypass rules for ICs. Most designs also have a bypass cap right at the oscillator of 0.01 or 0.02 uF. Bypassing the oscillator is wise because these devices not only have the noise margin problems, but they are driven in a sensitive and active loop during operation.

Most, if not all, metal DILs have a small 0.01 bypass chip capacitor internally and do not need additional bypassing. The Plastic SMD and DIPs are constructed almost like a monolithic IC, therefore placing chip caps inside is a real problem, especially for the high temperature SMD parts. These devices should have external bypass caps added. The very low frequency tuning fork types operating in the 25 kHz, as for the 18-18800 require about 0.2 uF bypass depending on the application

4.6.4 Package Outlines:

Figure 4-7: Plastic SMT Package

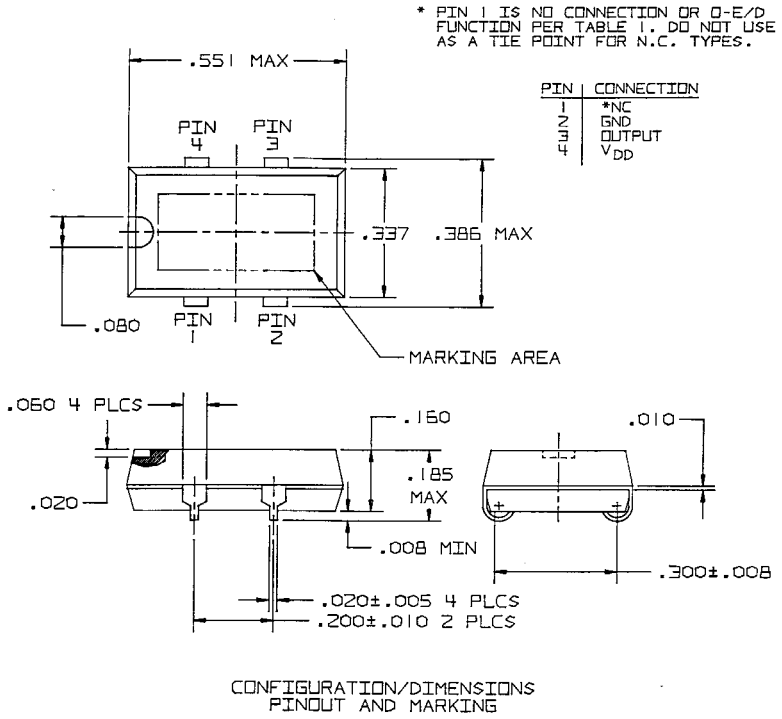


Figure 4-8: Plastic DIP Package

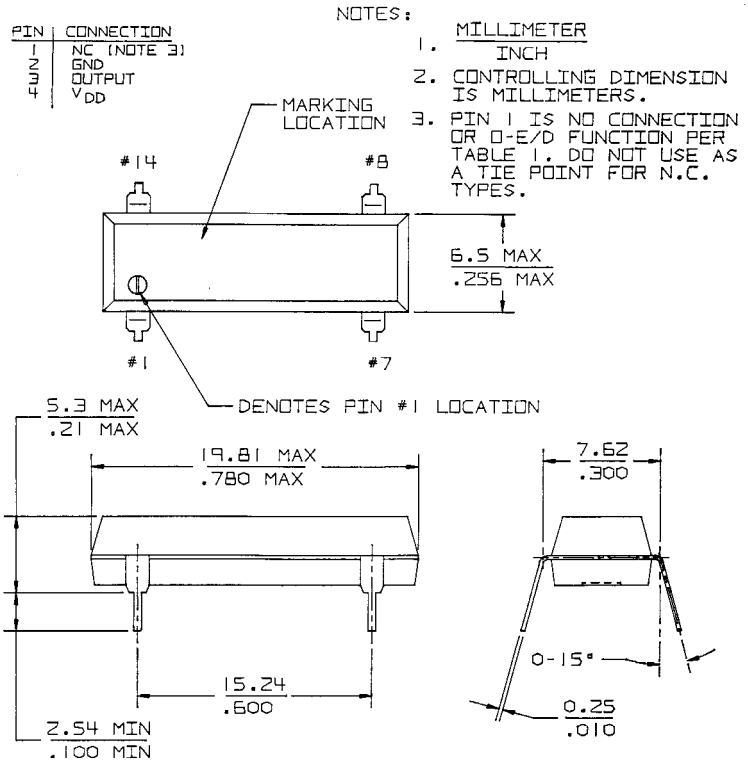
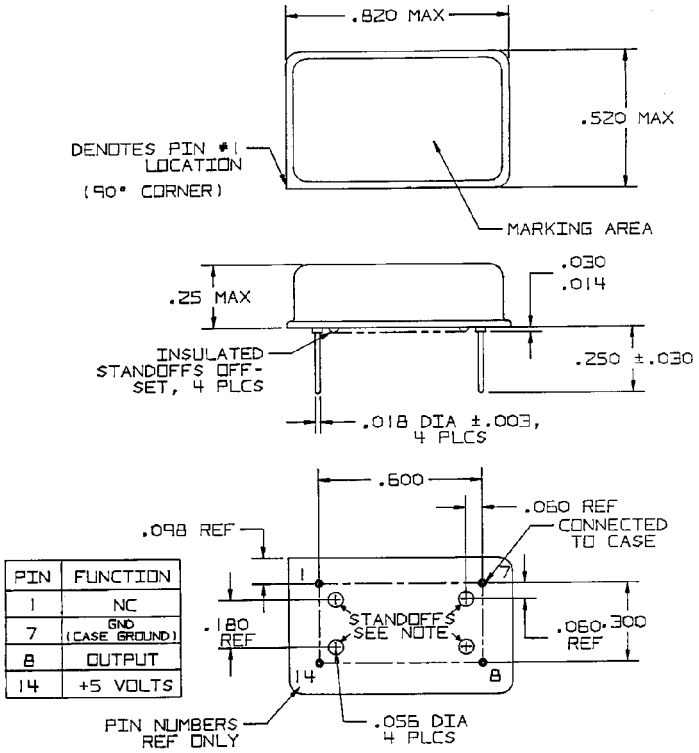


Figure 4-9: Metal DIL Package



4.7 Hybrids

As a family of components, hybrid circuit FCD codes are grouped by manufacturing process rather than specific subcomponent technology. Various configurations of hybrids range from simple resistor / capacitor passive networks to complex multiple semiconductor technology on the same substrate. Hybrid circuits may be found in Digital component classes 13, 19, 20, and 57. All of these hybrids will be grouped within the hybrid FCD codes described below within the technology matrix. Most of the digital-type hybrid circuits being purchased by Digital today utilize either thick or thin film substrate interconnect technologies. Power hybrids used in power supply applications are utilizing the direct bonded copper or Berquist interconnect methods.

4.7.1 Hybrid Circuit Selection/Specification Guide

Most hybrid circuits purchased by Digital are custom in nature. Hybrids generally provide the designer smaller space and faster response or specialized circuitry not easily achievable using standard component module technologies. The Digital designer makes hybrid process and technology selections only because the circuit schematics are normally Digital custom.

The Digital design engineer has several package, technology and attach methods available to choose from to meet the project cost, performance and space requirements. Each of these selections can affect the previously mentioned requirements.

4.7.1.1 Selection/Design Criteria

- **Technology required?** Hybrid circuits can provide ECL, TTL, CMOS, GaAS, power or mixed technology on the same substrate.
- **Substrate Process Technologies:**

Table 4-51: Hybrid Substrate Process Technologies

Attach	Interconnect	Substrate
SMD	Thick Film	Ceramic
Chip and Wire	Thick/Thin Film	Ceramic
Through-hole	Copper Etch	PCB
Flip-Chip	Thin Film	Ceramic
Power	Direct Bonded Copper	Ceramic
	Berquist	Al
	Thick/Thin Film	Beryllium

— **Power Hybrids:** Power hybrids use standard hybrid assembly techniques utilizing assembly materials capable of handling higher currents than required. Substrate technologies include heat spreading techniques**.**

- **Hybrid Package Attach?** Surface mount or through-hole.
  - — Package Integrity:
  - — Hermetic - Welded and capable of passing Mil-Std fine leak tests
  - — Nonhermetic lidded - Capable of passing Mil-Std gross leak test. (Normal Digital requirements)
  - — Potted - Package types for standard dc/dc converters and some communication hybrids available from supplier catalog
  - — Conformal Coated - Components sealed by applied conformal coating
- **Reliability:** FIT rate must be determined by modeling and actual in circuit measurements.
- **Suppliers:** Hybrid supplier selections are made based upon hybrid process type requirements. Each FCD code has approved suppliers with a proven process track record.
- **Specifications:** The hybrid general specification (20-00001-GS) sets general requirements. Hybrid specific specification sets specific requirements for each hybrid circuit.

4.7.2 Hybrid Preferred Parts

Due to the custom nature of these devices, there are currently no preferred parts identified.

4.7.3 Hybrid Design Guide

Table 4-52 shows the range of hybrid devices currently available.

Table 4-52: Comparison Matrix:

FCD	Technology	Appli-cation	Cost ($) Min/Typ/Max	Packaging	Reliability Considerations
NC1-NC7	Chip and Wire Thick/Thin Film	Custom	10 / 25 / 100	No Standard Package Size SIP / DIP / SMT	Nonhermetic /Hermetic High Temp Solder
NS1-NS7	SMD Thick Film	Custom	6 / 25 / 100	No Standard Package Size SIP / DIP / SMT	Nonhermetic Conformal Coated High Temp Solder
ND1-ND7	Mixed logic Thick/Thin Film	Custom	6 / 25 / 100	No Standard Package Size SIP / DIP / SMT	Nonhermetic /Hermetic High Temp Solder
NA1	DC-DC Converter 1-100 Watts	Stan-dard/ Custom	8 / 30 / 100	Package Size by Family Through-hole leads	Nonhermetic High Power May require heat sink
NA2	DC-DC Converter 100-199 Watts	Stan-dard/ Custom	75 / 130 / 175	Package Size by Family Through-hole leads	Nonhermetic High Power May require heat sink
NA3	DC-DC Converter 200-299 Watts	Stan-dard/ Custom	160 / 230 / 260	Package Size by Family Through-hole leads	Nonhermetic High Power Requires heat sink

4.7.3.1 Packaging

- Surface Mounted (SMT) Package Attach Versus Through-hole

Custom hybrid packages have traditionally utilized through-hole type leads as the attach method to the Digital module. SMT attach has become the standard for small outline, low power hybrids such as RC networks. Pick and place has traditionally been a problem with hybrids due to their lack of standard package sizes and the lack of a smooth surface on the top surface of the package. Because of these restrictions, most hybrids are hand inserted into the Digital module or application.

- Package Dimensions

Hybrid package dimensions are nonstandard and are usually customized to the particular requirements and design needs of the Digital application. Physical dimensions and design criteria for individual hybrid circuits are described generally in the 20-00001-GS and specifically in the detail purchase specification.

- High Power Applications

Power hybrids are traditionally used in Digital power systems or distributed power dc to dc converter applications. Power hybrids generally expend power in excess of 6 watts and can easily be in the >100 W range. Existing switching power supply designs are moving into the area of power hybrids because of the potential advantages of higher achievable switching frequencies and obvious space savings. High power hybrid applications are using direct bonded copper or the Berquist design of circuit substrate interconnect to meet the higher circuit current requirements and also to provide a higher level of circuit power dissipation.

4.7.3.2 Assembly Implications

- Standard Pin Spacing / Leads

Pin spacing for both plated through-hole and SMT type hybrid lead frames parallels the integrated circuit industry, but is not limited to these restrictions. Hybrid leads can be as custom as the hybrid itself. Pin requirements are specified within the 20-00001-GS and specifically in the detail purchase specification.

- Heat Sink Requirements

Hybrid package height restrictions are dictated by the Digital project design engineer. Many hybrid circuits require a heat sink to dissipate heat. Hybrid heat sinks must pass an attachment integrity and shear tests as described within 20-00001-GS. Heat sink attach materials must meet or exceed thermal dissipation and environmental stress testing as described in 20-00001-GS and required in the detail purchase specification. All bottom mounting hybrid circuits require a package stand off of 0.032 inch to allow cleaning and drying between the hybrid circuit and the Digital module.

- Size Restrictions

A hybrid mechanical stress study should be performed after mounting to a Digital module. Large hybrids using ceramic substrates are susceptible to cracking due to mechanical and thermal stresses. The level of concern depends upon the dimensional size of the hybrid substrate, its compliant ability, its location on the Digital module and the type and thickness of the hybrid substrate material used. Hybrid circuits can contain dissimilar materials that have different thermal coefficient of expansion than Digital module materials or other components used on the module. Any hybrid using a ceramic substrate greater than 1 inch square should provide its own mechanical stress relief.

- Hybrid Package Requirements—Hermeticity

All hybrid circuit assemblies purchased by Digital should be lidded or encapsulated to provide physical protection for components and resistance to corrosion and metal migration. External metalization shall be corrosion resistant or be plated or treated to prevent migration. Exposed metals containing silver are not allowed.

- Manual Assembly for Certain Hybrids

Hybrid circuits rated "NOT COMPATIBLE FOR DEC MFG." must be inserted and attached to

the Digital module or application by manual assembly techniques after the other components have been attached and the module has been cleaned. The term "NOT COMPATIBLE FOR DEC MFG." pertains to the thermal stresses applied during the solder attach process and/or the moisture penetration of the aqueous wash process.

4.7.3.3 Electrical Design Data

- Resistor Trim and Standard Tolerances

Active trim is performed on critical electrical parameters with the hybrid circuit in full or partial electrical operation. It compensates for differences in components used in the total affected circuit. Resistor material shall withstand > 50 watts per square inch after trimming according to 20-00001-GS.

Passive Trim is performed on individual resistors. 5% and 1% resistors are easily obtainable using standard thick film resistor inks. Resistor material shall withstand > 50 watts per square inch after trimming per 20-00001-GS.

- AC / DC Test Requirements

AC/DC test correlation on custom hybrids must be performed between Digital and the hybrid supplier on critical specified design test parameters. This activity must be completed prior to completion of component qualification.

4.7.3.4 Reliability Considerations

- Early Life Failures

The hybrid supplier must guarantee quality and reliability requirements stated in 20-00001-GS and detail component specification.

- Impacts of Storage and Shipping

Long term storage of hybrids in nonhermetic packages can be a concern. Long term storage of hybrid circuits (greater than 90 days) in normal storage (stock room) type environments can degrade solderability of hybrid leads. Moisture penetration is also a long term storage concern in environments with relative humidity > 40%. Long term storage should be in a nitrogen environment. Individual hybrid circuit assemblies shall be able to withstand short term shipping storage environments without physical or permanent damage with a relative humidity up to 95% over a temperature range of -40°C to +125°C.

- User Process Failures

Hybrids which fail during the Digital manufacturing process are the highest percentage of failures. Hybrids are more fragile but are generally handled in similar fashion as other nonautomatic insertable components.

- Expected Incoming Quality Levels

Most hybrid circuits purchased by Digital are custom and complex in nature. The 20-00001-GS establishes the incoming quality level at < 1000 ppm for the entire hybrid family. Incoming quality level for all hybrids on ship-to-stock is < 300 ppm.

4.7.3.5 Cost Data

- Custom Hybrids

Most hybrids purchased by Digital are custom. (Designed to a Digital proprietary schematic and specific application). For this reason, the cost is high. Average cost of custom hybrids purchased by Digital today is $30. An average nonrecurring engineering charge (NRE) of $10K is expended to establish a hybrid with a current AVL supplier. Average design cycle time from payment of NRE to receipt of prototypes is 6-10 weeks, depending on circuit and process complexities.

- Standard Product

Standard product hybrids are ordered from a supplier catalog. Examples of these would be dc to dc converters, RF amplifiers, and FET transistor arrays. NRE costs for standard product hybrids is very low or nonexistent. Part cost is normally 40–50% of similar custom circuits.

4.8 Optical Semiconductors

There are basically two types of optical semiconductors. They are:

1. Emitters/transmitters (visible, invisible or infrared)
2. Photodetectors/receivers are mostly infrared detectors and take many forms—diodes, transistors, integrated circuits

Optical devices are available in surface mount and through-hole packages. Displays and opto-couplers are in dual-inline packages and in surface mount SOIC packages. Table 4-53 lists the FCD codes and descriptions.

Table 4-53: Opto Device FCD codes

FCD	Description
B2A	Red LEDs
B2B	Green LEDs
B2C	Yellow LEDs
B2D	Multiple Colors
B2E	Numeric and Alphanumeric Displays
B5	Opto-couplers
B6	Opto-encoders, Interrupters

4.8.1 Opto Device Selection Criteria

- Devices should be selected from the preferred parts list. Preferred parts and their characteristics are listed in the tables that follow.
- Industry standard devices should be selected. As with any semiconductor, power dissipation, operating junction temperatures and operating voltage should be as low as possible to enhance life time and reliability.
- In order to select the correct visible LED/display, the following factors should be considered:
  - — *DEC STD 105-0 Display Workstation Ergonomics (Human Factors): Design Criteria* states that the colors/wavelengths shown in Tables 4-54 and 4-54 are to used for specific front panel (operator used indicators) applications.

Table 4-54: Colors of Push Buttons and Their Meanings

Color	Meaning Of Color	Typical Applications
Red	Action in Case of Emergency	Emergency Stop Firefighting
	Stop	General Stop To Stop one or more motors To Stop part of a machine or to Stop the cycle. (If the operator pushes the button during the cycle, the machine stops after the relevant cycle is completed.)
	Off	To open a switching device reset combined with Stop
Yellow/ Amber	Intervention	Intervention to suppress abnormal conditions or to avoid unwanted changes
Green	Start	General Start To Start one or more motors To Start a part of a machine or
	On	To close a switching device
Blue	Any specific meaning not covered by above colors	A meaning not covered by the colors Red, Yellow, and Green can be allocated to this color in particular cases.
Black/ Gray/ White	No specific meaning assigned	May be used for any function except for buttons with the sole function of Stop or Off.

Table 4-55: Colors of Indicator Lights and Their Meanings

Color in Peak Wave Length ±5nn	Meaning of the Lighted Indicator	Explanation
Red 620 nm and above	Danger or Alarm	Warning of potential danger or a situation that requires immediate (corrective) action
Yellow/Amber 580-590 nm	Caution (or write protect)	Change or impending change of conditions
Green 500-560 nm	Safety	Indication of a safe condition or authorization to proceed—clear way
Blue 420-290 nm	Specific meaning assigned according to the need in the case considered	Blue may be given any specific meaning that is not covered by the three colors Red, Yellow, and Green

Note that front panel operator indicators should be diffused-light devices with wide viewing angles (>90 degrees). Intensity/brightness should be considered for the application. Hazardous / dangerous indicators need to be readily seen.

4.8.2 Optical Semiconductor Preferred Parts

Table 4-56: Red LEDs (FCD B2A)

Part Number	Rating	Current	FY93 Cost ($)	Cost Trend	AVL Supplier	Lens Shape/Color	Case
11-29934-03	1MCD	2mA	0.07	Flat	Hewlett Packard	Round/Red	5 mm
11-27194-01	3MCD	10mA		Flat	Hewlett Packard	Square/Red	2X2 mm
11-14136-01	1MCD	5V/6mA	0,31	Flat	Dialight	Round/Rectangle/ Red	2 mm Block
11-17373-01	1MCD	20mA	0.13	Flat	Dialight	Round/Rectangle/ Red	5 mm Block
11-22809-01	1MCD	10mA	0.185	Flat	Dialight	Round/Rectangle/ Red	3 mm Block
11-16622-00	5MCD	20mA	0.09	Flat	Hewlett Packard	Rectangle	1X3 mm
11-18504-02	5MCD	10mA	0.06	Flat	Hewlett Packard	Round/Red	5 mm

Table 4-57: Green LEDs (FCD B2B)

Part Number	Rating	Current	FY93 Cost ($)	Cost Trend	AVL Supplier	Lens Shape/Color	Case
11-29934-01	2MCD	2mA	0.07	Flat	Hewlett Packard	Round/Green	5 mm
11-27194-03	3MCD	10mA		Flat	Hewlett Packard	Square/Green	2X2 mm
11-14136-02	1MCD	5V/5mA	0.31	Flat	Dialight	Round/Green	2 Mm Block
11-17373-00	2MCD	20 mA	0.13	Flat	Dialight	Round/Rectangle /Green	5mm Block
11-22809-02	1MCD	10mA	0.185	Flat	Dialight	Round/Rectangle /Green	3 mm Block
11-16622-02	3MCD	20mA	0.09	Flat	Hewlett Packard	Rect/Rectangle /Green	1X3 mm Block
11-18504-01	12MCD	20mA	0.055	Flat	Hewlett Packard	Round/Green	5 mm

Table 4-58: Yellow LEDs (FCD B2C)

Part Number	Rating	Current	FY93 Cost ($)	Cost Trend	AVL Supplier	Lens Shape/Color	Case
11-29934-02	1MCD	2mA	0.07	Flat	Hewlett Packard	Round/Yellow	5 mm
11-27194-02	3MCD	10mA		Flat	Hewlett Packard	Square/Yellow	2X2 mm
11-14136-03	1MCD	5V/5mA	0.31	Flat	Dialight	Round/Yellow	2 mm Block
11-17373-02	2MCD	20mA	0.13	Flat	Dialight	Round/Rectangle/ Yellow	5 mm Block
11-16622-01	5MCD	20mA	0.09	Flat	Hewlett Packard	Rectangle/Yellow	1X3 mm
11-18504-03	12MCD	10mA	0.005	Flat	Hewlett Packard	Round/Yellow	5 mm
11-38938-01	12MCD	10mA	0.38	Down	Dialight (Surface-Mount Device)	Round/Rectangle/ Clear	3 mm Block

Table 4-59: Multiple Color LEDs (FCD B2D)

Part Number	Rating	Current	FY93 Cost ($)	Cost Trend	AVL Supplier	Lens Shape/Color	Case
11-23142-01	1MCD	10mA	.329	Flat	Siemens	Red/Green	5 mm
11-31224-01	1MCD	20mA	1.08	Flat	Dialight	Rectangle, G/G/G	5 mm Block
11-31224-02	1MCD	20mA	1.04	Flat	Dialight	Rectangle, G/G/Y	5 mm Block
11-31224-05	1MCD	20mA	1.09	Flat	Dialight	Rectangle, G/Y/G	5 mm Block
11-31224-08	1MCD	20mA	1.23	Flat	Dialight	Rectangle, R/Y/G	5 mm Block
11-31224-03	1MCD	20mA	1.31	Flat	Dialight	Rectangle, G/G/G/G	5 mm Block
11-31224-04	1MCD	20mA	1.31	Flat	Dialight	Rectangle, G/G/G/Y	5 mm Block
11-31224-06	1MCD	20mA	1.31	Flat	Dialight	Rectangle, R/Y/R/R	5 mm Block
11-31224-07	1MCD	20mA	1.09	Flat	Dialight	Rectangle, Y/R/R	5 mm Block
11-31224-09	1MCD	20mA	1.00	Flat	Dialight	Rectangle, X/Y/G	5 mm Block
11-39326-01	7MCD	20mA	0.79	Down	Dialight	Vt, Rectangle, G/G	4 mm Block
11-39326-02	6MCD	20mA	0.79	Down	Dialight	Vt ,Rectangle, G/Y	4 mm Block
11-39326-03	6MCD	20mA	0.79	Down	Dialight	Vt, Rectangle, G/R	4 mm Block
11-39326-04	6MCD	20mA	0.79	Down	Dialight	Vt, Rectangle, Y/G	4 mm Block
11-39326-05	6MCD	20mA	0.79	Down	Dialight	Vt, Rectangle, R/G	4 mm Block

Table 4-60: Numeric/Alpha-Numeric Displays (FCD B2E)

Part Number	Description	FY93 Cost ($)	Cost Trend	AVL Supplier	Lens Shape/Color
19-11297-00	Single Character	0.55	Down	Hewlett Packard	0.3 in Character, Common Anode
19-31605-03	Single Character	0.60	Down	Hewlett Packard	0.3 in Character

Table 4-61: Opto-Couplers (FCD B5)

Part Number	Rating	Current	FY93 Cost ($)	Cost Trend	AVL Supplier	Applications	Case
19-17366-01	CTR=100% MIN	1V, 3mA	0.59	Flat	Siemens	Darlington Out	6 Pin DIP
19-21337-01	CTR=50% Min	10V, 10mA	0.50	Flat	Siemens, Motorola	Regulatory Approved	6 Pin DIP
19-21337-02	CTR=100-300%	10V, 10mA	0.50	Flat	Siemens, Motorola	Regulatory Approved	6 Pin DIP
19-21337-03	CTR=100-200%	2.5V, 5mA	0.45	Flat	Siemens, Motorola	Regulatory Approved	6 Pin DIP
19-21337-04	CTR=100-200%	2.5V, 5mA	0.45	Flat	Siemens, Motorola	Regulatory Approved	6 Pin DIP
19-22364-01	CTR=50% Min	10V@5mA and 10mA	0.75	Flat	Siemens	8KV Isolation V	4 Pin DIP

Table 4-62: Encoders, Interrupters (FCD B6)

Part Number	Description	FY93 Cost ($)	Cost Trend	AVL Supplier	Case
19-19958-01	Air Gap Interrupter	1.69	Flat	Optek	Assembly
11-22949-01	Reflective Interrupter	1.49	Flat	Optek	4 Pin Assembly
17-02621-01	Tape Sensor Assembly	6.92	Flat	Optek	Assembly
19-31657-01	2-Channel Encoder Assembly	12.50	Down	Hewlett Packard	Assembly

4.8.3 Optical Semiconductor Design Guide

4.8.3.1 B2A, B2B, B2C, B2D: Light Emitting Diodes, Red, Green, Yellow

CAUTION: Light emitting diodes, visible and infrared, are not to be observed under magnification/microscope when activated as injury to eyes can be caused by the concentrated beams of energy.

The color of the light emitted by the semiconductor (the wave length of the light) is determined by the semiconductor materials used to form P-N junction. Photons are emitted when a forward current flows through the P-N junction.

The intensity or brightness of the light is determined by multiple factors including forward current shape and material of plastic used for the body of the device and die construction and materials.

4.8.3.2 FCD B2E: Displays

These devices use the same semiconductor die materials as the listed FCDs but multiple dies are used and arranged such that when illuminated, they form segments of numbers/letters.

4.8.3.3 FCD B5: Opto-Couplers

An opto-coupler is made up of an infrared emitter and a detector arranged such that the emitted light, when turned on, will lie on the photosensitive area of the detector and cause the detector, if a diode or a transistor, to turn on. Turning the emitter off stops the light from hitting the photosensitive area of the transistor diode and the diode/ transistor turns off. Detectors and emitters are arranged in the same package such that they are aligned with each other.

4.8.3.4 FCD B6: Opto-Interrupters/Encoders

There are two types of optical interrupters—reflective type and air gap type. Both devices are used to detect mechanical motion. Both types have an IR emitter and a detector.

In the reflective device, the emitter transmits its energy to a surface outside the device package and if the surface is at a particular distance (focal point), the energy gets reflected back to the detector and turns the detector on. The air gap interrupter has its emitter facing the detector so that energy is transmitted through the air and falls onto the detector turning it on. If the beam of energy is interrupted by something (blocking the beam), the detector flag turns off.

Encoders are used to generate pulses which indicate speed and direction, usually of motors. Normally the encoder will have two interrupters placed side by side, and a circular mylar disk with small slots cut into it spins in the air-gap between the pairs of emitters and detectors. The slots allow the IR energy to go through to the detectors turning them on, while the material of the disk blocks the energy, turning the detectors off. The first detector to turn on, indicates direction. The frequency of the pulses indicates speed/position of the motor that has the disk attached to it.

4.8.3.5 Major Parameters - FCD B2A, B2B, B2C, B2D: LEDs

Forward Voltage Drop VF at a Specified Forward Current, IF. Reverse Leakage Current IR @ Specified Reverse Voltage, VR. Maximum power dissipation, maximum forward current, minimum reverse breakdown voltage.

Color is dependent on the radiated spectrum of the LED. Peak wavelength (λ)pk, and dominant wavelength (λ)d are the two parameters which describe the spectrum. Peak wavelength is that wavelength at the peak of the spectrum. It is maintained within narrow limits. The human eye detects differences in intensity (usually cannot detect a difference more sensitive than 2:1) and color differences. The dominant wavelength (λ)d is a quantitative measure of the color of an LED as perceived by the eye. The dominant wavelength is not necessarily dependent upon peak wavelength. (λ)d is that wavelength when mixed with an equal amount of light from a 6500°K lamp (the 6500°K color temperature source produces light which simulates the daylight produced by an overcast sky, will be perceived by the eye as the same color as is produced by the radiated spectrum of the LED.

Color = Dominant wavelength in nano meters. Intensity = Brightness in millicandella. Intensity

is proportional to the forward current (IF) flowing through the PN junction of the LED. Diffused and undiffused LEDs. For a LED which is assembled with a clear plastic the light output is a beam of light concentrated in a narrow radiation pattern. The device has a narrow viewing angle (θ). These types of devices used for back lighting applications where a beam of light travels through space and illuminates a front panel font. By adding diffusant to the plastic (metal particles, and so forth), the light beam will get diffused and the result would be a widening of the viewing angle. This light beam pattern is also somewhat dependent on the shape of the lens of the body of the LED (emitting surface). A bullet shaped LED will focus the beam of light whereas a flat top LED will diffuse the light beam.

4.8.3.6 Major Parameters—FCD B2E: Displays

LED displays are arrays of LEDs arranged in particular patterns such that by illuminating certain LEDs an outline of light shaped as a number, letter, or other character is produced. Some displays have integrated circuits included with drivers, decoders and memory such that a BCD or ASCII input logic levels will enable or turn on certain characters. Such devices are called *Intelligent Displays*. In most applications, there are multiple character or digit displays and the different characters/digits are strobed (turned on and off alternately) at high frequencies so that the human eye does not detect the blinking characters. The major parameters of these devices include all parameters of B2A, B2B, B2C and B2D plus parameters such as segment color and brightness match. If ICs are incorporated, a *truth table* would be given which would show input/output response.

4.8.3.7 Major Parameters—FCD B5: Opto-Couplers

Major parameters include forward voltage drop VF at specified forward current IF for the infrared LED. Also reverse leakage current IR @ specified VR. The output characterization varies with the type of output device: Diode, transistor, logic, gate, Schmidt trigger, thyristor and so forth. For all devices, a coupled transfer ratio (CTR) will also be specified by stating an input LED current and an appropriate output response. As follows:

Diode = Input LED current/output current = IF (LED)/IF(output diode)

Transistor = Input LED current/output transistor collector current IF(LED)/IC

Logic Gate= Input LED current/voltage output low = IF(LED)/VOL

These devices also have isolation voltage ISO, specified between input and output (all input pins shorted together and all output pins shorted together) and test voltage is applied between input and output.

Switching times response between input LED and output device are also specified.

4.8.3.8 Major Parameters—FCD B6: Interrupters, Encoders

The air gap and reflective interrupters and the encoders all have the same types of parameters as the opto-couplers. These devices are very similar in circuit/device types. The difference between FCD B5 and B6 devices is that the B5 output device is detecting conditions of the input LED. The output device for the B6 is detecting a motion between the input LED and the output.

Chapter 5: Connectors

This chapter provides guidelines to be used by hardware designers in the selection and application of connectors for module, backplane and associated cable use. The chapter is generally subdivided as follows:

- Connector component definition and selection
- Preferred Part Listings (PPLs) and recommended applications
- Connector related design consideration

As with other components, the 12 class connector types are subdivided into application families called Functional Class Descriptor (FCD) codes and are listed in the Specs-On-Computer (SPOC) data base that provides detailed data that can be accessed by Digital or supplier part number and FCD code. Each part number includes the following data:

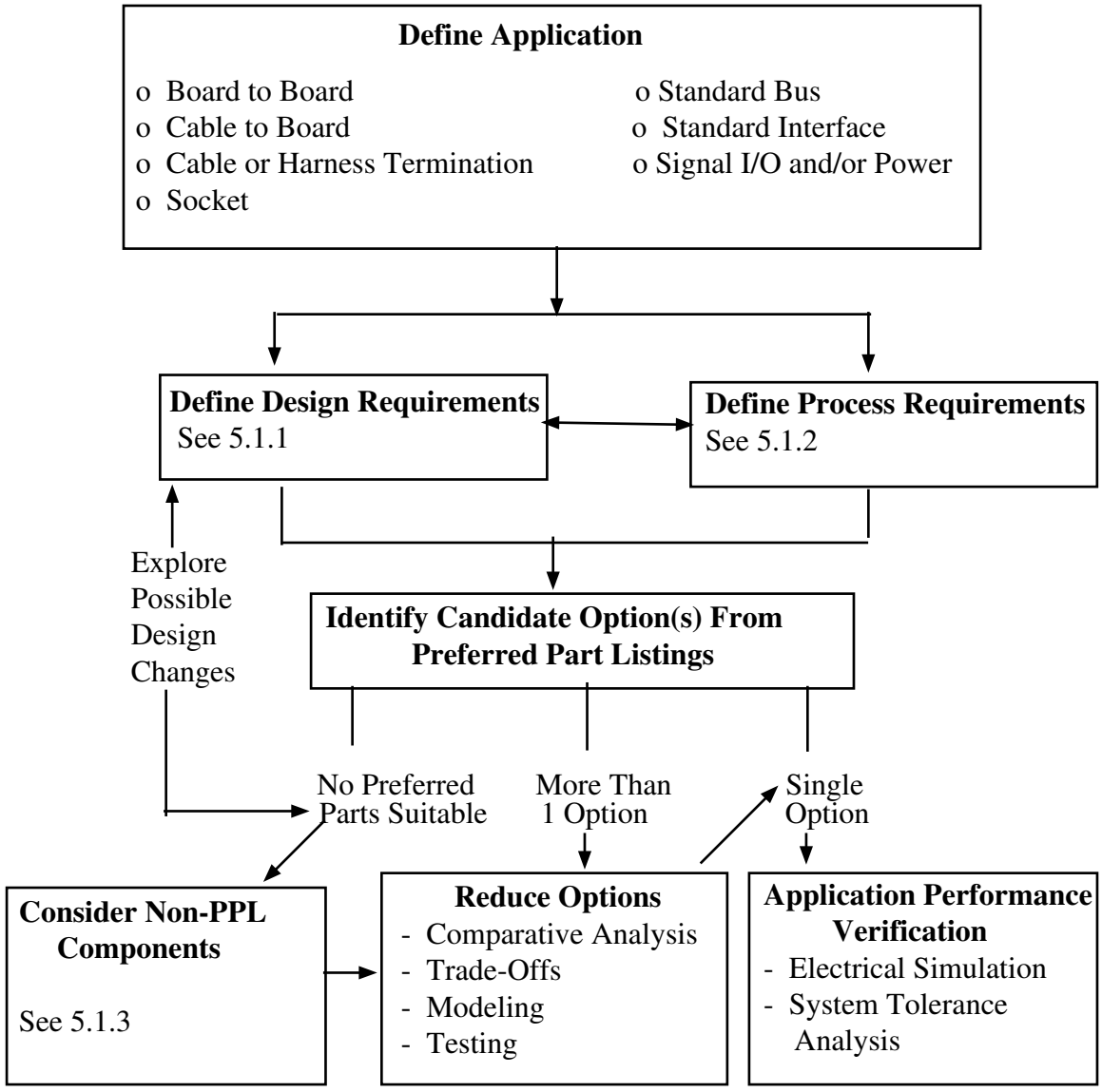
- Cost
- Type (Card Edge, Headers, Receptacles, and so forth)
- Part description (Number of contacts, pitch, rows, metallurgy, and so forth)
- Part drawings and revision status
- Supplier(s)
- Supplier part number
- Qualification status (qualified, under evaluation, risky, conditional)

SPOC lists many parts not covered in the PPLs. Many of these parts are still used to support older and existing products but are not included in the PPLs because they do not meet one or more of the selection criteria noted above.

5.1 Connector Component Definition And Selection

Figure 5-1 provides a generalized model for component definition and selection.

Figure 5-1: Component Definition and Selection



5.1.1 Definition of Design Requirements

The following is a checklist of design requirements that should be established prior to selecting a connector component.

- Pin count (signal, reference, power).
- Male component with non-active pins or female component with active receptacles.
- Orientation of interconnecting components (straight, 90°).
- PC board attributes (thickness, available footprint, headroom, active component clearance)
  or
  Cable attributes (AWG).
- Power requirements (voltage, current).
- Electrical performance (impedance, output risetime, crosstalk).
- Cost target.
- Shielding.
- Hardware (keying, latching).
- Product life.
- Operating environment (controlled computer environment versus uncontrolled).
- Durability (number of mate-unmate cycles).
- Contact metallurgy (tin, gold, palladium-nickel-gold).
- Reparability.

5.1.2 Definition of Connector Attachment Process Requirements

The following is a checklist of connector attachment options and considerations for PC board mount, and cable or harness termination, that should be established prior to selecting a connector component:

- PC Board Mount Options

Through Hole Wave Soldering		
Application	**Advantages**	**Disadvantages**
- Single sided through hole - Mixed technology - side 1	- Lowest component cost - No additional process	- Incompatible with side 2 component attachment

Selective Wave Soldering (Wenesco)		
Application	**Advantages**	**Disadvantages**
- Side 2 attach of through hole components - Selective side 1 attach	- Permits selective attach on sides 1 and 2	- Lower process yield - High process cost

Press Pin		
Application	**Advantages**	**Disadvantages**
- Compatible with all SMT designs - Side 2 attach	- High Yield process - No additional thermal excursion - Easily repaired - Low operating cost	- Additional process step - Additional equipment needed

Surface Mount		
Application	**Advantages**	**Disadvantages**
- Miniature design - All SMT design	- Small form factor - High volume SMT - One pass process - Increased routing potential	- Limited availability - Potential size limitation - Process not fully developed - Sensitive to rugged application

- PC Board Process Considerations
  - — Machine insertable
  - — Board retention features (kink tails, board locks, and so forth)
  - — Polarization/orientation features
- Cable or harness termination
  - — Solder
  - — Crimp
  - — Insulation displacement
  - — Molded vs. manufactured assembly

5.1.3 Considering Non-PPL Components

DO discuss the requirement with one of Digital's many technical support personnel. These personnel are resident in the Canadian Technology Center or the Component Engineering group and can assist in ensuring that all of the options provided by the preferred parts have been explored. If a new component is indicated, representation from New Product Purchasing and Commodity Management for Connectors should be involved.

DO NOT involve a Connector Vendor or embark on the introduction of a new component, or *special configuration* of an existing component, without first discussing the requirement with a Digital connector specialist.

In order of precedence:

1. Explore possible design changes. A minor relaxation may result in considerable cost savings, particularly if a new component or process is indicated.

2. Consider a variant of a component listed in the PPLs. Some variants exist in the SPOC data base for PPL connector types but are not listed due to inactivity, or because they have been added since the latest update of this document. New variants to existing component types can generally be added by Component Engineering with minimal cost and time.

3. Consider a non-preferred part listed in the SPOC data base. SPOC lists many parts not included in the PPLs. Many of these are still used to support older products but do not meet all of the PPL selection criteria.

4. Consider introduction of a new component.

- Restrict the introduction of new connectors to:
  - — meet widely used industry standards
  - — reduce cost
  - — enhance performance
- Evaluate the hidden costs incurred by new component types:
  - — NRE tooling charges
  - — performance evaluation and design development
  - — component qualification
  - — process development
  - — lead time for above

- Avoid special configurations if possible.
- New Component Introduction should:
  - — conform to the EPWG strategy
  - — be usable across several products
  - — anticipate future product needs

5.2 Preferred Part Listings and Recommended Applications

All connectors in the following Preferred Part Listings (PPLs) meet most or all of the following criteria.

- The connector is an industry standard , off-the-shelf part.
- The connector is an existing Qualified Part used in Digital.
- Manufacturing Processes to support manufacturing assembly exist in one or more Digital facilities.
- Performance is consistent with state-of-the-art for typical applications.
- Vendor(s) are on Approved Vendor List (AVL) and ideally are multiple source.

The following terminology and abbreviations are used throughout the PPL tables.

- All units are in inches unless otherwise specified.
- Rows/Contacts indicate the number of contact rows and *total* contacts. For example, 2/44 signifies 2 rows of 22 contacts for a total of 44 contacts.
- Tin signifies tin or tin-lead plating.
- Gold signifies a gold over nickel plating system.
- Pd-Ni signifies a palladium-nickel-gold plating system.
- CC = center-to-center distance of adjacent pins.
- Cont = the separable contact portion of the connector.
- Trmn = PC board termination (solder tail, press pin) for each contact.
- Ortn = Orientation (straight versus 90°).
- AWG = American Wire Gauge.
- Polrzd = Polarizing feature included.
- Ejctr = Ejector levers included.

5.2.1 BUS Connectors

a) EISA —188 Contact, Double Sided, Card Edge 12-33538-01

b) FUTUREBUS+

	Headers			
	Straight		90°	
	Solder Tail	Press Fit	Solder Tail	Press Fit
Signal	12-37877-XX	12-33433-XX	(1)	(2)
Power	(1)	12-33430-XX	(2)	(2)

	Receptacles			
	Straight		90°	
	Solder Tail	Press Fit	Solder Tail	Press Fit
Signal	(3)	(2)	12-33431-XX	(3)
Power	(2)	(2)	12-33432-XX	(3)

(1) Catalog item not presently used in Digital.

(2) Not available in the industry.

(3) In development by one or more suppliers.

c) HIPPI —Not currently used in Digital products.

d) MCA —90 Contact, Double Sided, Card Edge 12-39839-02

—112 Contact, Double Sided, Card Edge 12-39839-01

—240 Contact, Double Sided, Card Edge 12-39839-03

e) PCI —116 Contact, Double Sided, Card Edge 12-39839-??

—120 Contact, Double Sided, Card Edge 12-39839-??

—180 Contact, Double Sided, Card Edge 12-39839-??

—184 Contact, Double Sided, Card Edge 12-39839-??

?? indicates that variants of this part number have not yet been assigned.

f) PCMCIA —68 Pin, Two Piece, Industry Standard Component

—Vendor selection and qualification to be completed by Q3, FY93.

—Contact ICOE Component Engineering

g) SCSI-1

Interconnect	Male		Female		IDC Cable Panel Mount Female
	Straight	90°	Straight	90°	
I/O	Standardized external cable	Standardized external cable	(1)		12-27483-XX
Internal Device	Supplied on drive	Supplied on drive	Cable with 12-31024-03 or 12-23995-05		N/A

h) SCSI-2

Interconnect	Male		Female		IDC Cable Panel Mount Female
	Straight	90°	Straight	90°	
I/O	Standardized external cable	Standardized external cable	(1)	12-32088-XX	12-36930-02
Internal Device	Supplied on drive	Supplied on drive	Cable with 12-31024-03 or 12-23995-05		N/A

i) SCSI-3 — Under evaluation. Contact Bill Ham. Use VTX ELF for the latest location information.

j) TURBOCHANNEL

Headers			
Straight		90°	
Solder Tail	Press Pin	Solder Tail	Press Pin
12-32091-01	12-29892-01	12-28244-02	(1)

Receptacles			
Straight		90°	
Solder Tail	Press Pin	Solder Tail	Press Pin
12-32089-01	12-29890-01	(1)	(1)

(1) Catalog item not presently used in Digital

k) VME

Headers		Receptacles	
Straight		90°	
Solder Tail	Press Pin	Solder Tail	Press Pin
12-32089-01	12-29890-01	12-28244-02	(1)

(1) Catalog item not presently used in Digital

l) XMI — 5 Segment (60 positions per segment), ZIF, board mount. 12-26455-01
— Not a recommended component for applications other than XMI..

5.2.2 Standard Interface Connectors

Networks:

ETHERNET - Unshielded	12-33219
- Shielded Twisted Pair	12-33220
- Thin Wire	12-30221
- Thick Wire w/slide latches	12-30225
FDDI - Standard	24-35934
- Standard	24-35672
- Bayonet ST - Transceiver	24-33423
	(new) 24-35960
- Bayonet ST - Receiver	24-33424
	(new) 24-39988
TOKEN RING - Unshielded	12-33219
- Shielded, Twisted Pair	12-33220
- 9-Pin D-Sub (alternative)	12-29963-03

Storage:

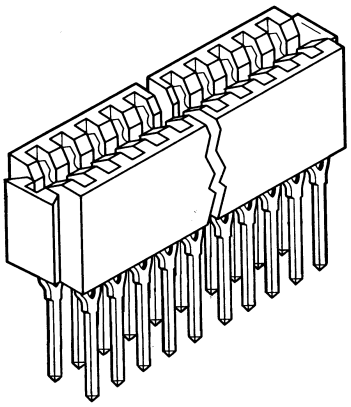
DSSI - IDC, Panel Mount, Male	12-31301-01
FDI - Floppy Disc	12-23627-03
IDE - PC Hard Disc	12-23627-04

Peripheral Devices:

SERIAL - No Modem (6 pin MMJ)	12-23433
- Modified Modem (9 pin D-Sub)	12-29963-01
- Full Modem (25 pin D-Sub)	12-29963-02
PARALLEL - 25 pin D-Sub	12-29963-02
MOUSE - 6 pin Mini-DIN	12-34934-05
- 7 pin Mini-DIN	12-26589
KEYBOARD - 6 pin Mini-DIN	12-34934-05
- 4 pin MMY Telephone Jack	12-18826
VIDEO - Monochrome - Preferred (15 pin D-Sub)	12-30225
- Alternative (BNC)	12-30221
- Color Graphics - Preferred	12-33080-02
- Alternative (BNC)	

5.2.3 Card Edge (FCD 1C)

- Primarily used for board-to-board applications.
- Largely being replaced by two piece pin and socket type connectors for increased density and performance applications.
- Available in solder tail and press pin for PC board mount application
- Gold plated spring beam contacts in the connector housing mate to gold plated fingers or pads on the edge of a mating PWB. These may be arranged in single or double rows depending on density.
- Available in 0.156, 0.125, 0.100 and 0.050 inch contact pitch.
- Preferred parts are restricted to 0.100 pitch except for a single power connector component which has 0.0125 pitch.
- Extensively used and are generally inexpensive.
- Use restricted in Digital to 0.057 to 0.115 inch thick PC boards for solder tail components and 0.084 to 0.200 for press pin components.



2 Sided, Card Edge

With Press Pin And Extended Posts

Table 5-1: Card Edge

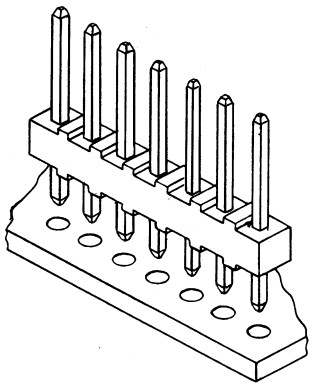
Number of Contacts	Attach Method	CC (Inch)	Plating		Tail Length (Inch)	Amps/ Pin	Notes	Digital Part Number	Costs $
			Cont	Trmn					
62 120	Solder	0.100	Gold	Tin	0.125 0.187			12-22993-01 -02	2.62 2.44
90 112 240	Solder	0.050	Gold	Tin	0.130	1	(1)	12-39839-02 -01 -03	
74 94 94	Press Pin	0.100	Gold	Tin	0.313 0.313 0.720			12-18421-04 -05 -03	4.36 3.01 2.72
36 72	Press Pin	0.125 0.125	Gold	Tin	0.230 0.230			12-26157-02 -01	2.12 1.76
60 120	Press Pin	0.100	Gold	Tin	0.189			12-31708-01 -02	3.03 3.98
188	Solder	0.50	Gold	Tin			(2)	12-33538-01	3.56
12	Crimp	0.100	Gold	Tin	N/A		(3)	12-30144-01	7.41

All above except 12-30144-01 are double sided components (mate with contact pads on both sides of PC board).

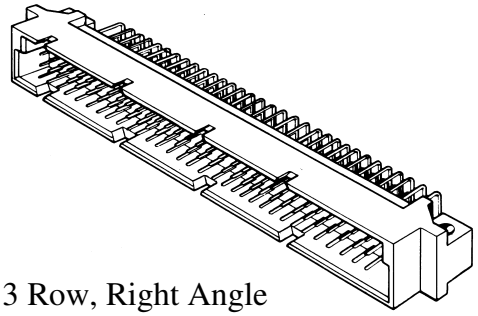
(1) MCA
(2) EISA
(3) Power Connector

5.2.4 Headers (FCD 1M)

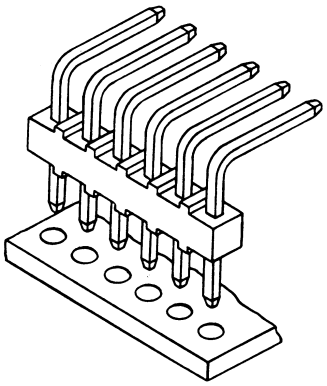
- Most common wire-to-board and board-to-board interconnect components, used for wide variety of applications including signal I/O, power, and test points.
- Non-active male pin component.
- Typically board mounted although cable mount types are available.
- Single or multi-row with 0.050, 2 mm, 0.100, 0.156, and 0.165 inch pitch being most common.
- Solder tail components available in straight or 90° configuration. Press pin components available only in straight configuration.
- Available as unshrouded or shrouded with one, two, three or four surrounding walls (for pin protection and mating alignment).
- Several polarizing schemes available.
- Mechanical latchings types available.
- Available in solder tail, press pin and recently SMT.



Single Row, Straight
Unshrouded Header



3 Row, Right Angle
DIN Header



Single Row, Right Angle
Unshrouded Header

Table 5-2: Headers - Solder Tail - Shrouded

Rows/ Contacts		CC (in)	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Ejctr	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn						
1 1 1	5 8 9	0.100	Tin	Tin	0.230	0.130	0.025	3	S	No	12-26557-04 -02 -05	0.18 0.23 0.24
1 1 1	4 5 6	2 mm	Pd-Ni	Pd-Ni	0.157	0.122	0.020	2	S	No	12-31920-02 -03 -04	0.15 0.18 0.38
1 1	8 10	2 mm	Pd-Ni	Pd-Ni	0.150	0.122		2	90°	No	12-33013-01 -02	0.45 0.55
2	14	0.165	Tin	Tin		0.137		6	90°	No	12-32009-01	1.76
2	10	0.165	Gold	Gold	0.230	0.137		6	90°	No	12-32010-01	6.68
2 2 2 2 2 2 2	10 20 26 34 40 50 50	0.100	Pd-Ni or Gold	Pd-Ni or Gold	0.230 0.230	0.150 0.150	0.025	1	S	Yes	12-15341-01 -09 -02 -06 -00 -05 -13	0.56 0.65 1.00 0.83 1.37 1.71 0.76
2 2 2 2	10 20 34 40	0.100	Gold	Tin	0.318	0.135	0.025	3	S	No	12-19952-06 -05 -01 -07	029 0.50 0.54 0.80
2 2 2 2	34 40 50 60	0.100	Gold	Gold	0.230 0.230 0.230	0.105 0.150 0.150	0.025	1	S	No	12-23627-03 -04 -01 -02	 0.98 1.16 1.33
2	60	0.100	Gold	Tin	0.125	0.100	0.015	1	S	No	12-31121-03	8.20

...Continued Next Page

Headers - Solder Tail - Shrouded - Cont'd

Rows/ Contacts		CC	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Ejector	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn						
2	120	0.100	Gold	Tin	0.240	0.165	0.025	1	S	No	12-31879-01	3.80
2	96	0.100	Gold	Tin	0.194	0.190	0.025	1	S	No	12-32091-01	1.67
2 2 2 2 2 2 2 2 2	6 10 14 20 34 40 50 50	0.100	Pd-Ni or Gold	Pd-Ni or Gold	0.230	0.105 0.150 0.150 0.105 0.105 0.105 0.105 0.150	0.025	1	90°	Yes	12-16832-01 -07 -11 -00 -06 -02 -03 -09	0.77 0.45 1.50 0.62 1.25 0.90 1.14 3.00
2 2 2	68 80 100	0.050	Gold	Tin	0.110	0.134	0.016 X 0.024	1	S	Yes	12-30006-01 -02 -03	2.59 2.66 3.18
2	96	0.050	Gold	Tin				1	S	No	12-33526-01	2.10
2	120	0.050	Gold	Tin				1	S	No	12-33790-01	
2 2	50 120	0.050	Gold	Tin		0.122		1	S	No	12-34720-02 -01	4.78 8.30
2 2 2 2	40 68 80 100	0.050	Gold	Tin		0.134	0.016 X 0.024	1	90°	Yes	12-29576-04 -01 -02 -03	2.65 2.76 3.08 4.09
2	120	0.050	Gold	Tin				1	90°	No	12-33794-02	6.08
3 (1)	96	0.100	Gold	Tin	0.250	0.104	0.025	1	90°	No	12-28244-02	2.08

S - Straight

(1) DIN - Mates to 12-32089-01.

Table 5-2.1: Headers - Solder Tail - Non-Shrouded

Rows/ Contacts		CC	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Locking Feature	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn						
1	1	0.100	Tin	Tin	0.318	0.215	0.025	3	S	No	12-12518-07	0.07
1	1		Gold	Gold	0.318	0.215					-19	0.07
1	1		Tin	Tin	0.230	0.195					-17	0.07
1	1		Tin	Tin	0.230	0.210					-05	0.32
1	2		Tin	Tin	0.230	0.195					-18	0.07
1	2		Tin	Tin	0.318	0.215					-09	0.06
1	2		Gold	Gold	0.318	0.215					-20	0.09
1	3		Tin	Tin	0.318	0.215					-11	0.09
1	4		Pd-Ni	Pd-Ni	0.318	0.215					-02	0.27
1	7		Tin	Tin	0.318	0.215					-03	0.10
1	9		Tin	Tin	0.318	0.215					-21	
1	23		Pd-Ni	Pd-Ni	0.318	0.215					-04	1.04
1	3	0.100	Tin	Tin	0.315	0.140	0.025	4	S	No	12-15816-01	0.08
1	8										-03	0.20
1	13										-02	0.33
1	15										-00	0.57
1	‘	0.100	Tin	Tin	0.200	0.095	0.025	5	S	No	12-15901-09	0.04
1	1		Tin	Tin	0.200	0.095					-01	0.06
1	1		Tin	Tin	0.230	0.120					-12	0.09
1	2		Gold	Gold	0.200	0.095					-06	0.08
1	5		Gold	Gold	0.230	0.095					-11	0.16
1	36		Tin	Tin	0.200	0.095					-00	0.53
1	2	0.100	Gold	Gold	0.295	0.140	0.025	2.5	S	Yes	12-14978-02	0.10
1	3					0.140					-03	0.15
1	4					0.135					-00	0.17
1	2	0.100	Tin	Tin	0.295	0.140	0.025	2.5	S	Yes	12-15323-02	0.05
1	3										-05	0.08
1	4										-01	0.09
1	6										-00	0.10
1	7										-04	0.12
1	9										-07	0.15
1	2	0.100	Gold	Gold	0.295	0.140	0.025	4	S	Yes	12-18243-02	0.11
1	3										-00	0.23
1	2	0.100	Tin	Tin	0.330	0.130	0.025	2.5	S	Yes	12-19251-00	0.05

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Headers - Solder Tail - Non-Shrouded - Cont'd

Rows/ Contacts		CC	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Locking Feature	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn						
1	2	0.100	Gold	Tin	0.295	0.140	0.025	4	S	Yes	12-27590-01	0.09
1	4										-07	0.21
1	6										-05	0.38
1	9										-10	0.39
1	10										-08	0.42
1	12										-02	0.71
1	15										-11	0.63
1	20										-04	0.83
1	24										-06	2.73
1	2	0.100	(1)	(1)	0.230	0.090	0.025	4	90°	No	12-14434-02	0.07
1	3	0.100	Tin	Tin							-09	0.11
1	3		(1)	(1)							-04	0.12
1	4		Tin	Tin							-10	0.11
1	6		(1)	(1)							-07	0.16
1	7		Tin	Tin							-16	0.13
1	7		(1)	(1)							-00	0.41
1	8		Tin	Tin							-15	0.15
1	8		Pd-Ni	Pd-Ni							-18	0.31
1	10		Tin	Tin							-17	0.23
1	16		(1)	(1)							-06	0.42
1	18		Tin	Tin							-08	0.31
1	5	0.100	Tin	Tin	0.295	0.135	0.025	2.5	90°	No	12-14981-04	0.12
1	2	0.100	Tin	Tin	0.260	0.143	0.025	2.5	90°	Yes	12-19196-03	0.17
1	3										-00	0.20
2	6	0.100	Pd-Ni	Pd-Ni	0.318	0.120	0.025	3	S	No	12-13488-01	0.26
2	10		or	or							-00	0.25
2	12		Gold	Tin							-06	0.29
2	16										-13	0.35
2	20										-02	0.53
2	50										-14	0.38

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Headers - Solder Tail - Non-Shrouded - Cont'd

Rows/ Contacts		CC	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Locking Feature	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn						
2	2	0.100	Gold	Tin	0.230	0.090	0.025	4	S	No	12-16862-06	0.11
2	6			or							-09	0.17
2	8			Gold							-07	0.23
2	8										-11	0.36
2	10										-02	0.29
2	14										-00	0.35
2	16										-04	1.34
2	22										-08	0.70
2	40										-01	1.00
2	50										-10	1.38
2	24	0.100	(1)	Tin	0.278	0.220	0.025	3	S	No	12-18292-03	1.09
2	10	0.100	(1)	(1)	0.230	0.095	0.025	4	90°	No	12-12965-01	0.23
2	12										-06	0.32
2	16										-07	0.49
2	20										-04	0.38
2	26										-03	0.55

(1) Pd-Ni or Gold

Table 5-2.2: Headers - Press Fit - Shrouded

Rows/ Contacts		CC	Plating		Pin Length		Pin Size	Amps/ Pin	Orntn	Ejctr	Notes	Digital Part Number	Cost $
			Cont	Trmn	Cont	Trmn							
2	6	0.100	Gold	Tin	0.320	0.180	0.025	3	S	No		12-17869-09	2.22
2	10											-04	2.77
2	16											-05	4.18
2	20											-01	2.04
2	26											-02	2.72
2	40											-00	2.84
2	52											-08	4.21
2	30	0.100	Gold	Tin or Gold	0.270	0.160	0.025	3	S	No		12-27111-01	1.42
2	10	0.100	Gold	Tin	0.230	0.175	0.025	3	S	Yes		12-20547-08	1.10
2	10											-13	1.33
2	14											-11	1.62
2	16											-14	1.56
2	20											-07	1.41
2	24											-15	3.07
2	30											-05	2.67
2	34											-06	1.64
2	40											-01	2.00
2	50											-16	2.50
2	50											-02	4.04
2	60											-09	4.70
3	120	0.100	Gold	Tin	0.210	0.210	0.025	3	S	No		12-28743-01	4.63
3	96	0.100	Gold	Tin	0.193	0.193	0.025	2	S	No	(5)	12-29892-01	2.25
3	45	0.100	Gold	Tin	0.241	0.241	0.025	1	S	No		12-31620-04	2.45
3	60											-03	3.25
3	60											-07	3.25
4	8	2 mm	Gold	Tin	(2)	(2)	.5 mm	2.75	S	No	(1)	12-33432-01	1.41
4	8											-02	1.57
4	24	2 mm	Gold	Tin	(4)	(4)	.5 mm	1.0	S	No	(3)	12-33433-02	1.05
4	24											-05	1.40
4	48											-04	
4	96											-03	5.55
4	192											-01	7.26

(1) 2 mm power segment (Futurebus).
(2) Available with pin lengths of 6.5, 7.25, and 8.0 mm. Termination 2.73 mm.
(3) 2 mm signal segment (Futurebus).
(4) Available with pin lengths of 6.5, 7.25 and 8.0 mm. Termination 2.73 and 3.53 mm.
(5) DIN. Mates to 12-32089-01.

Table 5-2.3: Headers - SMT

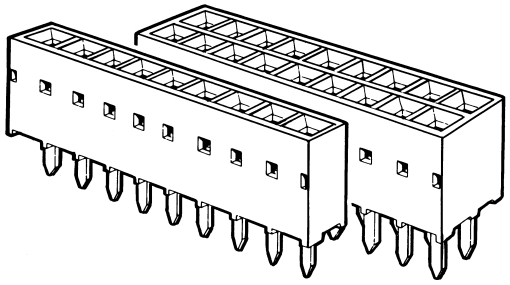
At the time of publication, there is limited use of SMT connectors in Digital, and preferred parts have not been established. Evaluation activities are in progress to:

- Identify current and near term product requirements for SMT connectors.
- Select currently available connectors which best meet these requirements.
- Assess the technical and economic impacts of using SMT connectors.
- If justified, develop processes for assembly and repair of these connectors for backplanes and modules.
- Develop a solder joint reliability model.
- Perform reliability assessment and qualification testing.

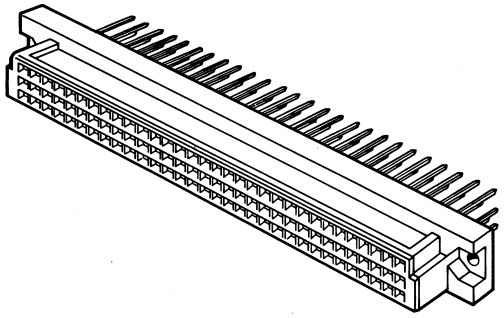
For status contact Steve Bonnell. Use VTX ELF for the latest location information.

5.2.5 Receptacles (PCB Mount Female) (FCD 1R)

- Used for board-to-board and cable-to-board applications requiring an active female receptacle component.
- Predominantly used for backplane applications with increasing use in motherboard or daughterboard applications.
- Predominantly in 90° configuration although vertical configurations such as DIN and stacking types are also used.
- Available in solder tail, press pin and recently SMT.
- Will play an important role in future development of improved signal integrity and higher density connector systems.



Single Row and Double Row,
Straight Receptacles



DIN, 3-Row, Solder-to-board,
Straight Receptacle

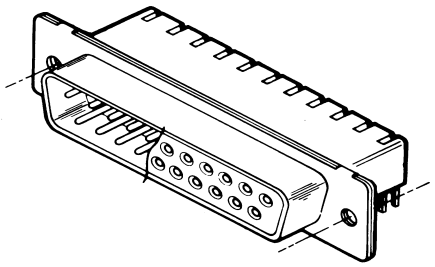
Table 5-3: Receptacles (PCB Mount Female)

Rows/ Contacts		Attach Method	CC	Plating		Tail Length	Orntn	Power Rating (Amps)	Notes	Digital Part Number	Cost $
				Cont	Trmn						
2	60	Solder	0.100	Gold	Gold or Tin	0.115	S	3		12-19065-08	3.24
2 2	96 96	Solder	0.050	Gold	Tin	0.134	S	1 1	(1)	12-33527-01 -02	4.95 4.10
2	120	Solder	0.050	Gold	Tin	0.134	S	1	(2)	12-34163-01	5.03
3	96	Solder	0.100	Gold	Tin	0.180	S	1	(3)	12-32089-01	1.70
4 4	8 8	Solder	2 mm	Gold	Tin	2.73 mm 3.53 mm	90°	2.75	(4)	12-33430-01 -02	1.02 1.02
4 4 4 4 4 4 4 4	24 24 48 48 96 96 192 192	Solder	2 mm	Gold	Tin	2.73 mm 3.53 mm 2.73 mm 3.53 mm 2.73 mm 3.53 mm 2.73 mm 3.53 mm	90°	1	(5)	12-33431-03 -04 -05 -06 -07 -08 -01 -02	0.93 0.93 1.90 1.50 3.42 5.90 5.90
2	50		0.050						(6)	12-32088 -07	8.50

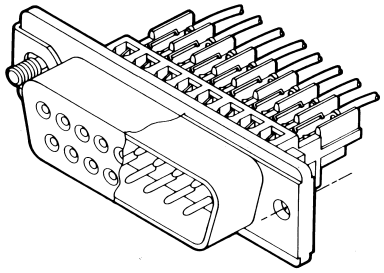
(1) Board-to-board stacking. Mates to 12-33526-XX.
(2) Board-to-board stacking. Mates to 12-34164-XX.
(3) DIN (Turbochannel). Mates to 12-29892-01.
(4) Power segment (Futurebus).
(5) Signal segment (Futurebus).
(6) SCSI.

5.2.6 Subminiature D (FCD 1P)

- Industry standard connector type named for its D shaped polarizing shell design.
- Available in male and female configurations.
- Extensively used for shielded cable interconnection between electronic enclosures — particularly serial communication area networks, telecommunication, and local area networks.
- Volume cable application is predominantly molded assemblies.
- Two series, HD-20 and HD-22, each have five sizes related to the size of the shell. Shell sizes numbered 1 to 5 are identical for both series.
- Depending on the size of the contacts, it is possible to have different numbers of contact cavities in a given shell size.
- Reference standards:
  - — MIL-C-24308.
  - — EIA Standard RS-32 (low speed serial communication) recommends 25 position connectors.
  - — ISO 2110 is the main International Standards Organization document
  - — IEEE 802.3 covers bus-structured LANs such as Ethernet using HDP-20 15 position connectors.
- The standard subminature D connector is a full metal-shell version using crimp, soldercup or posted contacts. Insulation displacement, front metal-shell, all plastic, shielded and filtered versions are available.
- A wide variety of shielded and unshielded cable clamps and associated hardware such as screw locks, locking posts and latching arrangements are available.



Subminiature D, Board Mount



Subminiature D, Cable Mount

Table 5-4: Subminiature D, Male - PCB Mount

Number of Contacts	Plating		Tail Length	Orientation	Attachment	Notes	Digital Part Number	Cost $
	Cont	Trmn						
15	Gold	Gold	0.125	Straight		(1)	12-21634-01	1.90
25	Gold	Tin		Straight	Insert		12-25898-01	1.66
50	Gold	Tin	0.188	Straight	Hole		12-31460-01	7.76
9	Gold	Tin	0.125	90°	Insert		12-29963-03	2.33
9 25	Gold	Tin	0.125	90°	Insert		12-26314-03 -01	0.38 0.80
15	Gold	Gold	0.125	90°	Insert		12-20398-02	1.28
15	Gold	Tin	0.125	90°		(1)	12-31021-01	1.25
15 25	Gold	Tin	0.125 0.125	90°	Standoff		12-33351-01 -02	1.60 1.80
50	Gold	Gold	0.125	90°	Insert		12-19679-07	3.78
50	Gold	Gold	0.125	90°	Standoff		12-28017-01	5.75

Table 5-4.1: Subminiature D, Female - PCB Mount

Number of Contacts	Plating		Tail Length	Orientation	Attachment	Notes	Digital Part Number	Cost $
	Cont	Trmn						
15	Gold	Gold	0.125	Straight	Hole		12-20350-01	1.95
15	Gold	Gold	0.125	Straight	Special	(1)	12-21808-01	3.90
25	Gold	Gold	0.160	Straight	Insert		12-24776-02	3.07
3	Gold		0.155	90°	Insert	(2)	12-33080-02	6.27
9	Gold	Tin	0.125	90°	Insert		12-35167-01	3.27
15	Gold	Tin	0.125	90°	Insert		12-25983-01	1.05
15	Gold	Gold	0.125	90°	Special	(1)	12-30225-01	1.99

Inserts and standoffs all 4-40 thread.
Hole - Denotes standard mounting hole 0.120 inch diameter.
(1) Special attachment, Ethernet application only.
(2) Video RGB, 75 ohm, 3 Coax in D-Sub shell.

Table 5-4.2: Subminiature D, Female - Cable Mount

Number of Contacts	Termination	Orientation	Attachment	Notes	Digital Part Number	Cost $
9 15 25 50	N/A	Straight	N/A	(1)	12-10493-52 -58 -32 -62	0.67 0.46 0.51
15	IDC	(2)	Hole		12-27940-01	2.32
50	IDC	(2)	Hole		12-20502-01	7.24

Table 5-4.3: Subminiature D, Male - Cable Mount

Number of Contacts	Termination	Orientation	Attachment	Notes	Digital Part Number	Cost $
3	N/A	Straight	N/A	(1)	12-35046-01	
9 15 25	N/A	Straight	N/A	(1)	12-10493-68 -57 -59	 0.46 0.61
25	IDC	(2)	Insert		12-29451-01	7.20
50	IDC	(2)	Insert		12-20808-01	8.43

IDC - Insulation Displacement

Hole - Denotes standard mounting hole 0.120 inch diameter

Inserts all 4-40 threads

(1) Housing only. Ref. Table 5-4.4 for contacts

(2) Orientation determined by wire dress.

Table 5-4.4: Subminiature D Housings - Contact Reference

Recommended sockets for female housing 12-10493-XX

AWG	Insulation Support	Material	Plating		Digital Part Number	Cost $
			Cont	Trmn		
24-20	Yes	Ph-Br.	Gold	Gold	12-10493-41	0.080
28-24	No	Ph-Br.	Gold	Gold	12-10493-45	0.043
28-24	Yes	Ph-Br.	Gold	Tin	12-10493-56	0.085

Recommended pins for male housing 12-10493-XX

AWG	Insulation Support	Material	Plating		Digital Part Number	Cost $
			Cont	Trmn		
24-20	Yes	Brass	Gold	Tin	12-10493-39	0.038
28-24	No	Brass	Gold	Tin	12-10493-43	0.039
28-24	Yes	Brass	Gold	Tin	12-10493-61	

Recommended pins for male housing 12-35046-01

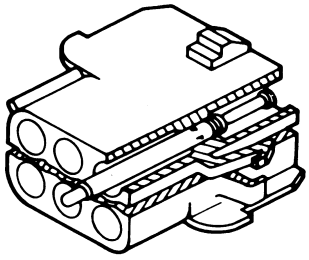
Wire Description	Impedance	Plating		Digital Part Number	Cost $
		Cont	Trmn		
Coaxial RG180 BU	75 ohms	Gold	Gold	12-35044-01	

All contacts listed above are crimp attach and in strip form.

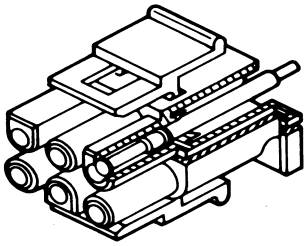
Ph-Br = Phosphor Bronze

5.2.7 Mate-N-Lock (FCD 1F)

- AMP trademark component.
- Used for cable or harness interconnection of current carrying lines.
- Panel mount PC board or free hanging configurations available.
- 2 to 15 line housings available.
- Pins and sockets can be intermixed in the same housing.
- Contacts completely enclosed in housing so pin or socket contacts can be hot.
- Positive locking housings.
- Innumerable keying combinations.
- Contacts accept 30-10 AWG wire sizes.
- Make first, break last capability using ground pins.
- Low contact mating force.
- Removable, crimp snap-in contacts.



6 Circuit Plug



6 Circuit Receptacle

Table 5-5: Mate-N-Lock - Headers

Rows/ Contacts		CC	Tail Length	Amps/ Pins	Mates To	Orientation	Type	Digital Part Number	Cost $
1	2	0.200	0.140	15 Max.	12-10821-02	Straight	C	12-11342-02	0.16
1	3		0.140		-03			-03	0.22
1	3		0.210		-03			-18	0.43
1	4		0.140		-04			-04	0.14
1	2	0.250	0.175	15 Max.	12-12168-01	Straight	U	12-12297-00	0.10
1	2				-01			-19	0.40
1	2		0.235		-01			-10	0.33
1	3		0.175		-00			-03	0.20
1	3		0.235		-00			-14	0.36
1	4		0.175		-02			-01	0.17
1	4		0.235		-02			-15	0.45
2	6		0.175		-05			-05	0.46
2	6		0.235		-05			-12	0.59
3	9		0.175		-07			-02	0.39
3	15		0.175		-06			-04	0.59
3	15		0.175		-06			-09	0.47
1	2	0.250	0.160	25 Max.	12-12168-01	90°	U	12-21027-02	0.52
1	3				-00			-01	0.44
1	4				-02			-03	0.63
1	5				-08			-05	1.03
					-12				
1	8				-10			-04	1.23

Table 5-5.1: Mate-N-Lock - Receptacle

Rows/ Contacts		CC	Tail Length	Amps/ Pin	Mates To	Orientation	Type	Digital Part Number	Cost $
1	2	0.250	0.175	15 Max.	12-12167-02	Straight	C	12-17485-00	0.13
1	3				-00	Straight		-01	0.17
1	2	0.250	0.160	25 Max.	12-12169-02	90°	(1)	12-28176-01	0.78

C - Commercial

U - Universal

(1) Mounting Ears

Tails are Tin plated throughout.

Table 5-5.2: Mate-N-Lock - Cable Mount - Male Housings

Rows/ Contacts		CC	Trmn.	Mates To	Contacts	M or F	Type	Digital Part Number	Cost $
1	3	0.200	Free	12-09350-XX	12-09378-XX	Male	C	12-09351-03	0.08
1	4		Hanging		or			-04	0.12
1	6				12-09379-XX	Female		-06	0.18
3	5							-15	0.35
1	1	0.200	Free	12-10821-XX	12-10821-XX	Male	C	12-10822-01	0.04
1	2		Hanging					-02	0.07
1	2	0.250	Free	12-12168-XX	12-12169-XX	Male	U	12-12167-02	0.06
1	2		Hanging		or			-17	0.30
1	3				12-12170-XX	Female		-00	0.07
1	4							-01	0.06
1	5							-11	0.20
1	5							-16	0.24
1	8							-13	
2	6							-06	0.13
3	9							-04	0.15
3	9							-12	0.10
3	12							-03	0.09
3	15							-05	0.19

C - Commercial

U - Universal

All above are crimp wire termination

Cost of contacts are extra

Table 5-5.3: Mate-N-Lock - Cable Mount - Female Housing

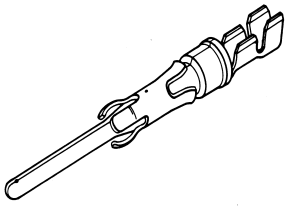
Rows/ Contacts		CC	Trmn.	Mates To	Contacts	M or F	Type	Digital Part Number	Cost $
1	3	0.200	Panel Mount	12-09351-XX	12-09378-X or 12-09379-XX	Male Female	C	12-09350-03	0.10
1	4							-04	0.10
1	2	0.200	Free Hanging	12-10822-XX or 12-10900-00 or 12-11342-XX	12-09379-XX	Female	C	12-10821-02	0.12
1	3							-03	0.08
1	4							-04	0.08
1	2	0.250	Panel Mount	12-12167-XX	12-12169-XX or 12-12170-XX	Male Female	U	12-12168-01	0.06
1	3							-00	0.06
1	3							-13	
1	4							-02	0.07
1	5							-08	0.24
1	5							-12	
2	6							-05	0.16
3	9							-07	0.23
3	9							-11	0.21
3	15							-06	0.22

C - Commercial U - Universal

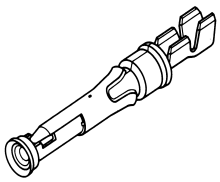
All above are crimp wire termination.

5.2.8 Pin and Socket (FCD 1O)

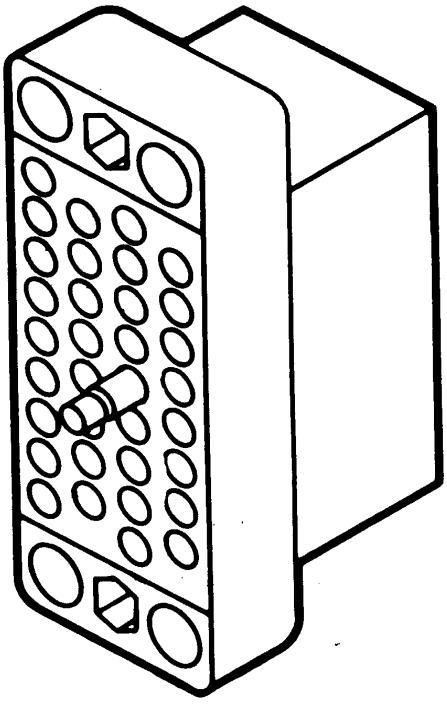
- Exclusively for wire and cable applications.
- Covers terminals (pin and socket types) as well as the housings that they are used in.
- Typical spacings of 0.050, 0.100, 0.125, 0.156, and 0.200 but may include other grid spacings.
- Free hanging and panel mountable.
- Accommodates various wire gauges, typically from 30 AWG to 14 AWG.
- Various pin diameters.
- Available in gold and tin.



Typical Pin



Typical Socket



Typical Housing

Table 5-6: Pin and Socket—Housings

Rows/ Contacts		CC	Height	Contact Part Number	Mates To	Digital Part Number	Cost $
1	2	0.100	0.500	12-14979-XX	12-15323-XX	12-15322-01	0.05
1	3					-04	0.05
1	6					-00	0.09
1	9					-08	0.13
1	13					-06	0.21
2	6	0.100	0.546	12-10089-XX	12-12220-XX	12-10918-34	
2	10					-32	0.35
2	14					-30	0.33
2	20					-27	1.84
2	24					-25	0.58
2	44					-15	0.86
2	20	0.100	0.545	12-10089-XX		12-17309-11	1.92
2	24					-00	0.95
2	54					-06	
1	2	0.156	0.660	12-25786-XX		12-26013-07	
1	3					-08	0.12
1	4					-03	
1	5					-02	0.14
1	6					-01	0.07
1	7					-13	
1	10					-11	
1	12					-09	
1	15					-12	0.41
1	3	0.165	0.921	12-37914-XX	12-37771-XX	12-37770-01	
2	6	0.165		12-28768-XX	12-30112-XX	12-30111-04	0.12
2	10			or	or	-02	0.12
2	12			12-30410-XX	12-29570-XX	-06	0.16
2	14				or	-01	0.13
					12-30159-XX		

Ref. Table 5- 6.1 for contact data.

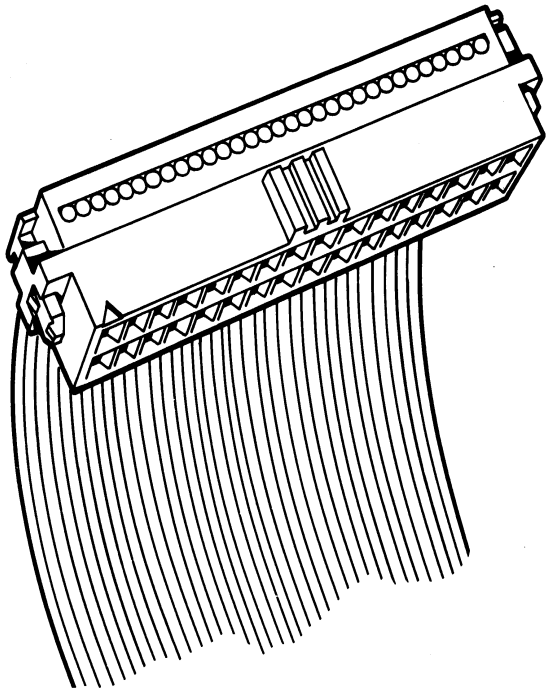
Table 5-6.1: Pin and Socket—Contacts

Digital Part Number	AWG	Plating	Amps	Package	Notes	Unit Cost $
12-10089-00	28-32	Gold	3	Reel		0.075
-05	22-28				(1)	0.075
-07	22-28				(2)	0.084
12-14979-00	22-30	Gold	3	Reel		0.027
-01	22-30	Tin		Reel		0.007
12-25786-01		Tin				0.016
12-28768-01	18-24	Gold	5	Reel		0.140
-03	18-24	Gold	5	Reel		0.091
12-30410-01	18-24	Tin	6	Loose		0.014
12-37914-01	18-24	Tin		Reel		

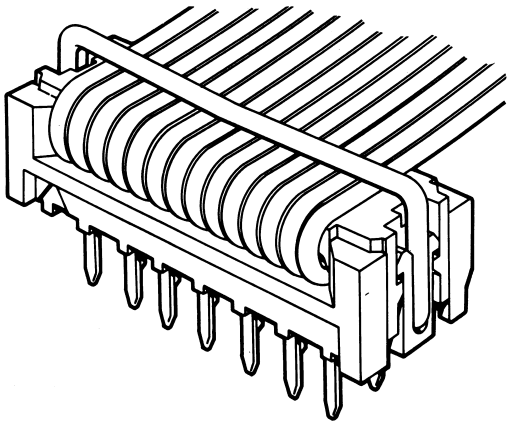
(1) 0.0035 Spring - Use if the total number of contacts equals or is greater than 19.
(2) 0.005 Spring - Use if the total number of contacts equals or is less than 18.

5.2.9 Insulation Displacement - IDC (FCD 1N)

- Used for cable and harness assemblies.
- Uses an insulation piercing type contact for wire termination, resulting in economical and reliable wire-to-connector termination.
- Used in a variety of connector styles including subminiature D.



IDC Receptacle



IDC Header

Table 5-7: Insulation Displacement - IDC - Female

Rows/ Contacts		CC	Mating Pin	AWG	Cover Type	Polrzd	Strain Relief	Notes	Digital Part Number	Cost $
1	9	0.156	0 .045	18	CL	No	No	(1)	12-15306-00	0.23
1	24	0.100	0.025	22	FT	No	No		12-17651-06	
1	2	0.100	0.025	22	CL	No	No		12-18296- 02	0.17
1	3			26					-08	
1	4			22					-01	0.47
1	5			22					-20	
1	6			22					-03	0.73
1	6			24					-12	
1	9			22					-05	
1	10			22					-25	
1	12			22					-23	
1	15			22					-26	
1	20			22					-21	
2	10	0.100	0.025	28	CL	No	Yes		12-19163-09	0.69
2	20				CL				-10	0.38
2	34				CL				-14	2.24
2	50				FT				-02	3.08
2	50				CL				-07	2.98
2	10	0.100	0.025	22-26	N/A	No	No		12-22126-06	
2	14			20-22					-03	2.64
2	16			20-26					-01	1.65
2	16			20-22					-04	2.00
2	20			20-22					-07	
2	24			20-22					-17	
2	26			22-22					-08	
2	30			20-26					-10	3.96
2	34			20-22					-16	
2	14	0.100	0.025	28	CL	Yes	Yes		12-22243-02	
2	30								-01	1.60
2	50								-03	

...Continued Next Page

Insulation Displacement - IDC - Female - Cont'd

Rows/ Contacts		CC	Mating Pin	AWG	Cover Type	Polrzd	Strain Relief	Notes	Digital Part Number	Cost $
2	10	0.100	0.025	28	FT	Yes	Yes		12-23995-02	0.55
2	16				FT				-06	1.03
2	20				FT				-03	0.50
2	24				CL			(2)	-15	0.51
2	26				FT				-07	0.19
2	30				CL				-09	
2	30				CL			(3)	-10	
2	34				FT				-04	2.28
2	34				CL			(3)	-16	
2	40				FT				-01	3.80
2	44				FT			(3)	-19	
2	50				FT				-05	0.88
2	60				FT				-08	5.25
2	50	0.050 X 0.100	0.016 X 0.024	28	N/A	Yes	No	(4)	12-29089-01	
2	40	0.050	0.016	28	N/A	Yes	No		12-29577-04	
2	68	X	X						-01	4.90
2	100	0.100	0.024						-03	2.32
2	68	0.050 X 0.100	0.016 X 0.024	28-30	N/A	Yes	No	(5)	12-30007-01	4.85
2	50			28	N/A	Yes	No	(6)	12-31302-01	7.96
2	50	0.050 X 0.100	0.016 X 0.024	30	N/A	Yes	No	(7)	12-36930-01	

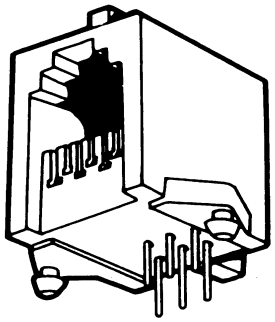
Table 5-7.1: Insulation Displacement - Male

Rows/ Contact		CC	Pin Size	AWG	Cover Type	Polrzd	Strain Relief	Notes	Digital Part Number	Cost $
2 2	50 50	0.100	0.025	28	FT	Yes	Yes	(8) (9)	12-28708-01 -02	3.28 6.27
2 2	50 50	0.050 X 0.100	0.016 X 0.024	28 30	N/A	Yes	No	(10)	12-29090-01 -02	4.97
2	68	0.050 X 0.100	0.016 X 0.024	28	N/A	Yes	No	(11)	12-29634-01	
2	50			28	N/A	Yes	No	(12)	12-31301-01	
2 2	50 100	0.050 X 0.100	0.016 X 0.024	28	N/A	Yes	No		12-32087-01 -03	
2	50	0.085 X 0.160			N/A	Yes	No	(13)	12-33601-01	

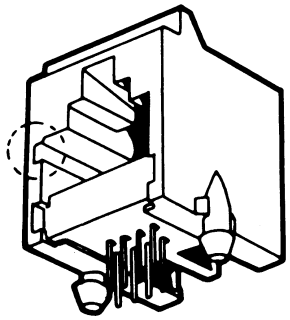
FT - Feedthrough
CL - Closed
N/A - Not applicable
(1) Power application, tin plating.
(2) Left entry.
(3) Right entry.
(4) Digital Storage Systems Interface (DSSI) - D shape.
(5) D shape. Mates to 12-29634-01.
(6) New DSSI - Micro Ribbon, cable mount, D shape. Mates to 12-31301-01.
(7) Panel mount, D shape. Mates to 12-32087.
(8) Ejector latches.
(9) Ejector latches and mounting flange.
(10) DSSI male, panel mount. Mates to 12-29089-01.
(11) Panel mount, D Shape. Mates to 12-30007-01.
(12) New DSSI - Micro Ribbon, panel mount, D shape.
(13) SCSI 1 -IEEE, ribbon style, D shape.

5.2.10 Telephone (FCD 1J)

- Standard receptacle and plug connectors used for I/O interconnect to peripheral devices such as keyboards and modems.
- Receptacle is typically board mounted, solder tail.
- Plug is typically wire/cable terminated.
- Available in 4 to 8 positions, straight or right angle, standard or low profile, and shielded or unshielded.



6 Position, PC Board Mount
Telephone Jack



8 Position, PC Board Mount
Telephone Jack, with key

Table 5-8: Telephone - PC Board Mount, Receptacles

Position/ Contacts		Tail Length	Orientation	Color	Mates To	Notes	Digital Part Number	Cost $
4	4	0.150	90°	Black	12-18831-XX		12-18826-00	0.78
4	4			Gray			-07	0.21
6	4			Black			-01	0.31
8	8			Black			-06	0.85
8	8			Gray		(4)	-09	5.55
6	6	0.150	Straight	Gray	12-23432-XX	(1)	12-23433-01	0.28
6	6		90°	Gray		(1)	-02	0.23
8	8	0.150	90°	Black	12-27854-02	(2)	12-33220-01	0.60

Table 5-8.1: Telephone - Cable Mount, Plugs

Position/ Contacts		AWG	Color	Mates To	Notes	Digital Part Number	Cost $
4	4	28	Clear	12-18826-XX		12-18831-00	0.16
6	6	28	Clear			-02	
8	8	26-28	Clear	12-18826-XX	(3)	12-27854-02	0.44
6	6		Clear	12-23433-XX	(1) (4)	12-23432-01	16.90
6	6		Clear		(1) (4)	-02	10.50

(1) LAN with offset latch.

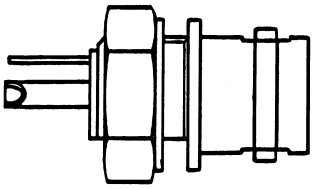
(2) Shielded, low profile, no keying.

(3) For round cable applications.

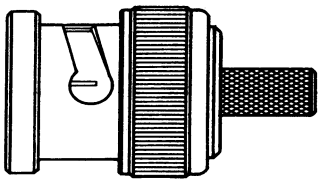
(4) Sold in packages of 50.

5.2.11 Coaxial (FCD 1B)

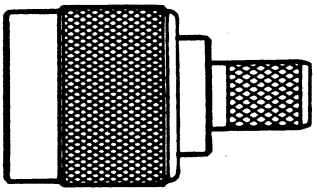
- Coaxial connectors are an integral part of coaxial cable assemblies used in RF transmission line application.
- Selection considerations include connector interface (BNC, TNC, and so forth), method of termination (PC board, cable, free hanging) and physical construction (MIL-type, commercial, plating, and so forth).
- Locking systems include Bayonet, Threaded, and Friction.
- Common types include BNC, TNC, SMA, and SMB although several less standard types are available.
- Termination of the connector to an RG cable can play an important role in the performance of a coaxial cable assembly.
- Cable termination generally consists of either soldered, crimped, or a combination of the two for the center conductor and the shield.



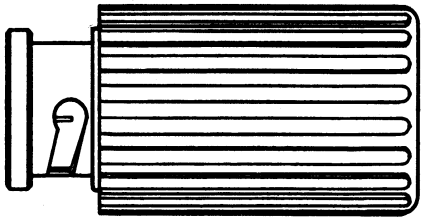
BNC Straight Bulkhead Receptacle with Ground Wire



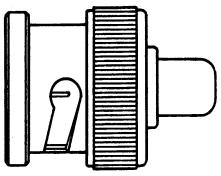
BNC Straight Plug with Wire Crimp



TNC Straight Plug with Wire Crimp



BNC Straight Terminator, Overmolded



BNC Straight Terminator

Table 5-9: Coaxial (BNC)

Male/ Female	Orientation	Tail Length	Cable Type	Electrical		Notes	Digital Part Number	Cost $
				Z	f_{max}			
M	Straight	N/A		50 ohms	4 GHz		12-25566-02	0.68
M	Straight	N/A	RG179B	75 ohms	2 GHz		12-27110-01	
M	Straight	N/A	N/A	50 ohms		(1)	12-26318-01	1.15
F	90°	0.187	N/A	50 ohms	11 GHz		12-25148-01	0.92
F	Straight	0.300	N/A	50 ohms	4 GHz		12-32818-01	1.53

Table 5-9.1: Coaxial (TNC)

Male/ Female	Orientation	Tail Length	Cable Type	Electrical		Notes	Digital Part Number	Cost $
				Z	f_{max}			
M	Straight	N/A	RG58	50 ohms	300 MHz		12-18647-00	1.64
M	Straight	N/A	RG179	75 ohms	7 GHz		12-32418-01	
M	Straight	N/A	N/A	50 ohms	300 MHz	(2)	12-18633-01	1.80
F	Straight	0.125	N/A	50 ohms	300 MHz		12-17979-01	3.20
F	90°	0.187	N/A	75 ohms	4 GHz		12-32419-01	3.10

(1) Terminator, Overmolded

(2) Terminator

5.2.12 Power (FCD 1H)

- Connectors identified in this section are for primary power distribution.
- Connector types for ac primary power are essentially defined and regulated by industry and safety standards.
- Used for high current carrying capabilities (> 1 amp).
- Both line cord and PWB connectors are available.
- Dedicated power connector configurations used for secondary power are included in other FCDs such as Card Edge, Headers, Receptacles and so forth.
- Mate-n-lock connectors are predominantly used for power applications. See subhead 5.2.7 for additional information.

Table 5-10: Power (FCD 1H)

Application	I	Type	T	Pins	Current Rating	Voltage Rating	Digital Part Number	Cost $
Panel Mount, Female	SI SI	IEC Type 320	F S	3	10A 15A	250ac 250ac	12-14157-06 -11	0.55
Panel Mount, Male	SI SM	IEC Type 320	F F	3	10A 10A	250ac 125ac	12-17874-03 -00	0.45 0.43
Cable Mount, Male, 30		NEMA Style L21-20P NEMA Style L21-30P	Sc Sc	5 5	20A 30A	120/280 120/280	12-11209-00 12-12314-00	4.54 4.84

I - Installation
SI - Snap In
SM - Screw Mount

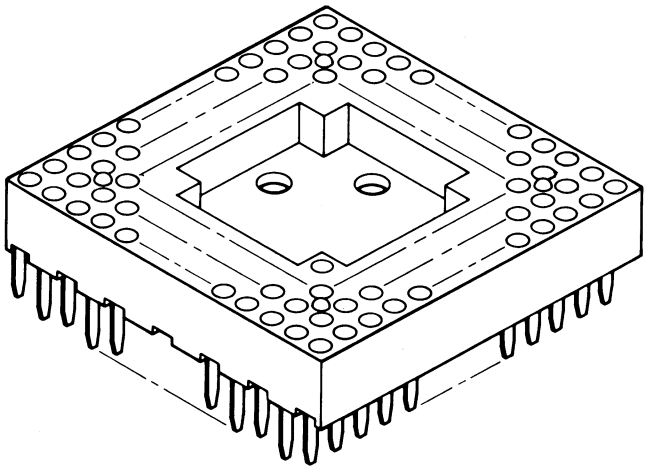
T - Termination
F - Faston
S - Solder
Sc - Screw
A - Amps

Table 5-10.1: Power Headers (Press Pin)

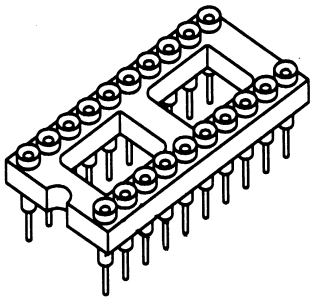
Current Rating	Voltage Rating	NumberTails/ Segment	Number of Segments	Tail Length	CC	Digital Part Number	Cost $
12.5A		5	1		0.100	12-23222-02	0.31
12.5A		5	1		X	-03	0.31
15A		6	1		0.300	-01	0.34
25A		10	1			-09	0.38
15A/Seg.		6	5			-05	2.25
15A/Seg.		6	5			-06	2.25
20A/Seg.		8	5			-04	2.17

5.2.13 IC Sockets (FCD 1I)

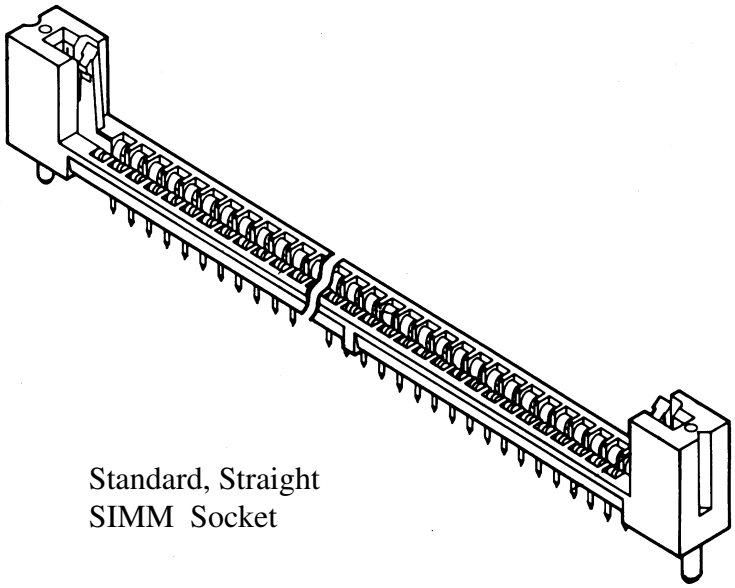
- PC board mounted components are used to create a separable interface for board mounted components such as PLCC, SIP, DIP, PGA, SIMM, and so forth.
- Most IC packages are controlled by JEDEC standards.
- Tin plating or gold plating is used in the contact area to match the plating selected for the mating components.



PGA Socket



Open Frame
DIP Socket



Standard, Straight
SIMM Socket

Table 5-11: DIP (Dual In-Line Package)

Number of Contacts	CC	Plating		Tail Length	Pin Dia	Height	Digital Part Number	Cost $
		Cont	Trmn					
24	0.100 X 0.600	Gold	Tin	0.107	0.023	0.155	12-12385- 04	0.25
28							-03	0.70
40							-00	1.01
6	0.100 X 0.300	Tin	Tin	0.120	0.024	0.195	12-15006-24	0.07
8	0.100 X 0.300			0.110			-00	0.05
14	0.100 X 0.300			0.130			-01	0.07
16	0.100 X 0.300			0.110			-02	0.08
16	0.100 X 0.300			0.130			-14	0.07
18	0.100 X 0.300			0.130			-15	0.19
20	0.100 X 0.300			0.110			-04	0.09
20	0.100 X 0.300			0.120			-22	0.11
24	0.100 X 0.300			0.110			-13	0.11
24	0.100 X 0.300			0.120			-23	0.13
24	0.100 X 0.600			0.110			-06	0.12
28	0.100 X 0.600			0.110			-07	0.13
28	0.100 X 0.600			0.130			-17	0.13
32	0.100 X 0.600			0.128			-25	0.15
40	0.100 X 0.600			0.110			-08	0.19
40	0.100 X 0.600			0.130			-18	0.18
48	0.100 X 0.600			0.120			-20	0.66
64	0.100 X 0.900			0.130			-19	0.88
24	0.100 X 0.600	Gold	Tin	?	0.020	0.183	12-19911- 01	0.93
28				0 .950			-05	0.65
28				0.125			-02	0.55
40				0.950			-06	0.92
48				0.950			-07	1.30
24	0.100 X 0.600	Gold	Tin	0.120	0.052	0.100	12-32339-01	1.22

Height = Board to socket clearance

Table 5-11.1: PGA (Pin Grid Array)

Number of Contacts	CC	Plating		Tail Length	Pin Size		Height	Outer Dimension	Digital Part Number	Cost $
		Cont	Trmn		PGA	PWB				
121	0.100 X 0.100	Gold	Tin	0.137	0.018	0.018	0.250	1.35 Sq.	12-24714-01	4.86
132	0.100 X 0.100	Gold	Tin	0.125	0.018	0.018	0.206	1.45 Sq.	12-33308-01	6.26
145	0.100 X 0.100	Gold	Tin	0.137	0.018	0.025	0.250	1.55 Sq.	12-27767-01	5.66
168	0.100 X 0.100	Gold	Tin	0.125	0.018	0.018	0.206	1.75 Sq.	12-33280-01	9.02
223	0.100 X 0.100	Gold	Tin	0.125	0.018	0.020		1.85 Sq.	12-30995-01	6.03

Table 5-11.2: PLCC (Plastic Leaded Chip Carrier)

Number of Contacts	CC	Plating		Tail Length	Pin Diameter	Height	Outer Dimension	Digital Part Number	Cost $
		Cont	Trmn						
32	0. 050	Tin	Tin	0.130		0.200	0.765 X 0.665	12-32911-01 -02	1.55 1.74
68 84	0.050	Tin	Tin	0.130	0.020	0.344	1.195 Sq. 1.395 Sq.	12-21158-01 -02	1.05 2.58
68 84	0.050	Gold	Tin	0.130	0.025	0.275	1.295 Sq. 1.495 Sq.	12-22185-02 -01	3.98 5.87

Height = Board to socket clearance

Table 5-11.3: SIMM (Single In-Line Memory Module)

Number of Contacts	CC	Plating		Tail Length	Orientation	Latch	Digital Part Number	Cost $
		Cont	Trmn					
72 80	0.050	Gold	Tin	0.120	Straight	Metal	12-34138-03 -01	1.94 2.06
72 80	0.050	Gold	Tin	0.120	22°	Metal	12-35432-02 -01	3.14 2.91
80	0.050	Gold	Tin	0.120	40°	Metal	12-40098-01	

Table 5-11.4: SIP (Single In-Line Package)

Number of Contacts	CC	Plating		Tail Length	Pin Diameter	Height (1)	Notes	Digital Part Number	Cost $
		Cont	Trmn						
3 8 10 13 13	0.100	Tin	Tin	0.145 0.145 0.145 0.130 0.145	0.025 Sq.	0.160		12-17535-04 -13 -01 -16 -05	0.35 0.33 0.34 0.25 0.27
8	0.100	Tin	Tin	0.126	0.020 Sq.		(2)	12-30766-01	0.27

(1) Board to socket clearance

(2) Right angle orientation

5.3 Connector Related Design Considerations

5.3.1 Contact Density

- Proportional to contact pitch.
- The contact density of a connector governs the number of contacts attainable per inch of an interconnecting structure such as a module edge.
- *Effective* contact density is expressed as the number of pins or lines per linear inch. For example a 4 row, 0.100 inch pitch connector has an effective contact density of 40 pins per inch.
- As packaging density increases and PC board real estate becomes more valuable, *true* contact density (pin per unit area of connector footprint) becomes more important.

5.3.2 Contact Plating

- For signal applications (typically currents less than 1 amp) choose gold or palladium plated contacts for optimal signal reliability.
- Plating thickness has a direct influence on the durability (number of mate/unmate cycles). Use of components with less than 30 microinches of gold should be carefully evaluated for the intended application.
- Do not mix gold and tin in mating connectors.
- Plating selection and thickness influences component cost.
- Tin plated contacts are predominantly used for power and less critical, cost sensitive applications.

5.3.3 Mating Force

- High pin counts can result in surprisingly high insertion forces.
- Consider the need for the generation of mating force with handles, injector tabs, and so forth.
- Consider the ability of adjacent componentry to withstand mating forces, for example card cage and backplane structural design or the need for a backplane stiffener.
- Lubrication is not recommended as a means to reduce insertion force due to its propensity to allow contamination to collect and adhere to the contact surfaces.

5.3.4 Housing Materials

- Ensure specified housing materials are compatible with any thermal exposure that the connector may have to withstand during manufacturing assembly.

5.3.5 Tolerances

- Carefully analyze the tolerance limits of a connector system with respect to any associated hardware, for example PC Boards, card cage, and card guides, as well as potential deflections due to insertion loads.

- Assure that assembly tolerance limits will not result in inadequate mating (wipe) and stubbing (interference of contacts pins or pads with mating componentry).

- Assure that specified tolerances are compatible with current manufacturing assembly process capabilities.

5.3.6 Footprint Clearances

- The connector housing, including mating parts and latching arrangements, define the connector footprint.

- Manufacturing and repair processes require additional clearance between the connector footprint and adjacent componentry on a PC board. Reference Rule 4-1, in Chapter 7, sub-head 7.3.4.

5.3.7 Sequencing

- Sequencing is typically used to assure that power ground and/or signal reference is in place before signal contacts are made.

- Contact pin lengths are varied within a connector housing to provide first make/last break situations. Some applications may require 2 or more levels of sequencing.

- A limited number of connectors have the capability of varying contact pin lengths.

- Usually means specifying a *special* component with cost implementations.

- In designing systems using sequencing connectors, special care must be taken to assure that system assembly tolerances do not negate the intended sequencing feature.

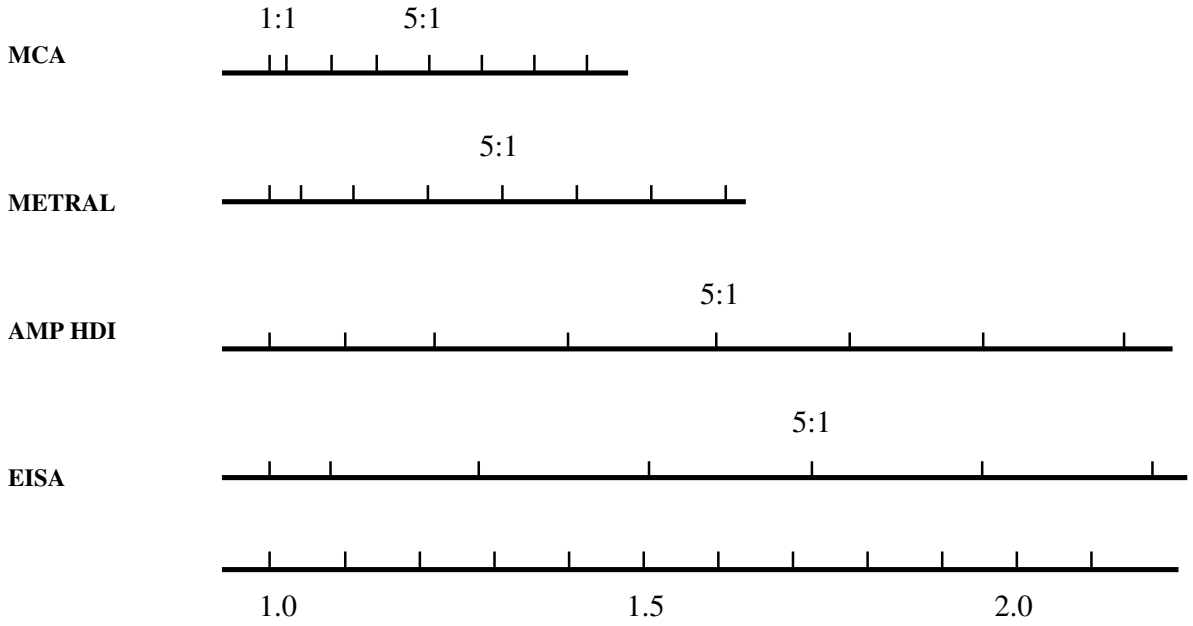
5.3.8 Electrical Performance Versus Cost Trade-Offs

- Cost per line is influenced by the type (physical construction) of a connector as well the

choice of signal-to-reference ratio.

- Use of high performance connector types:
  - — Is generally more expensive than use of reference pins.
  - — Is primarily used for controlled impedance applications.
- Use of reference pins for increased performance:
  - — Permits *selective* performance (reference Figure 5-2 Relationship Between Output Risetime and Sig: Ref. Ratio for an example).
  - — Is generally less expensive than use of high performance type connectors.
  - — Permits selective performance within a pin field.
  - — Permits use of reference pins to provide return path for power .
  - — Increases the cost per signal line.
  - — Reduces the effective contact density.

Figure 5-2: Relationship Between Output Risetime and Sig: Ref Ratio



5.3.9 Reparability

- Component repair, such as pin replacement, is possible in most connector types.
- Special tooling may be required.

5.3.10 Power (Current Carrying) Considerations

- Connector types for ac primary power are essentially defined and regulated by industry and safety standards.

- In electronic packaging, the use of power connectors versus the use of signal pins is a trade-off involving cost, the current carrying capacity of individual pins, heat loss considerations, and voltage drop budget.

- When choosing to use dedicated signal pins for power, an important consideration is the fact that any the signal reference pins parallel the function of the power return pins.

- Advertised current ratings can only be effectively used as an approximate guide to the actual capability of a connector applied to power handling. Most listed current ratings are based on temperature rise at a given current. However, individual mounting arrangements can significantly impact this rating depending on the current carrying capability of adjacent materials and structures (for example, via contact with bus bars, multiple or thicker power planes in a PWB, and so forth). Usually an *application specific* rating must be determined experimentally.

- In many applications, a critical parameter is the IR drop across the connector. In these cases, the amount of current that is allowed can be substantially lower than would be allowed based on temperature rise. This is one of the main reasons that contacts used for power are *derated* for certain system applications.

- When multiple pins are used in parallel, it is common practice to derate the current rating of the individual pin to accommodate the fact that some pins will usually carry more current than others.

5.3.11 Modeling And Simulation

For a specific application the electrical performance of a connector can be effectively predicted by modeling. Modeling is the process of converting the physical structure of a connector into an electrical circuit equivalent. Parameter extraction tools such as TDTL, RAMAP/ SITAP and EISOP can be used to expedite this process. These models can then be used in a circuit simulator such as SPICE to predict signal characteristics such as output risetime, propagation delay or crosstalk. Also, simulation is used to determine signal-to-reference ratio and geometric positioning of reference pins to signal pins for optimal signal performance.

Simulation of the power-carrying capabilities of a connector sees limited use because of the difficulty in determining the contact resistance of the separable interface. For this reason the values used in determining the elements in modeling the connector are usually derived empirically.

5.3.12 Factors Influencing Component Cost

- Use of preferred parts will increase volume buys and thereby facilitate cost reduction.
- Use of industry standard parts takes advantage of volume manufacture and competition between vendors to achieve lower costs.
- Use of customized (special) components usually incurs significant cost penalties due to non-recurring engineering charges, new or modified molds and/or assembly equipment.
- Sole sourced, non-standardized, non-intermateable components usually result in higher costs.
- Choice of materials such as low versus high temperature plastics or plating metallurgy (tin versus gold versus palladium-nickel) and thickness can significantly impact the cost of connector components.
- Complexities such as miniaturization with tighter tolerances or increased fragility can result in lower yields and thereby increase unit cost.
- Attachment method (wave solder versus selective solder versus presspin versus surface mount, or hand versus automated positioning and assembly) are factors that can influence the total assembled cost. Reference the Module Assembly Value Added Cost section in Chapter 10, (in process).

5.4 Glossary of Terms

DIP - Dual In-Line Package

EIA - Electronic Industries Association

EISA - Extended Industry Standard Architecture

HIPPI - High Performance Parallel Interface

IEC - International Electronic Commission

IPI - Intelligent Peripheral Interface

ISA - Industry Standard Architecture

JEDEC - Joint Electron Device Council

MCA - Micro Channel Architecture

PCI - Peripheral Component Interconnect

PCMCIA - Personal Computer Memory Card International Association

PGA - Pin Grid Array

PLCC - Plastic Leaded Chip Carrier

SCSI - Small Computer Storage Interface

SIMM - Single In-Line Memory Module

SIP - Single In-Line Package

VME - Versa Module Eurocard

XMI - Extended Memory Interface

5.5 Key Contributor

The following people were key contributors to this chapter:

Name	Responsibility	Organization
Stu Daughtrey	Chapter Captain	Canadian Technology Center
Dan Hassett	Component Engineering	Interconnect Center of Expertise
Fran Sleeper	Component Engineering	Interconnect Center of Expertise
Steve Perry	Data Search and Consolidation	Interconnect Center of Expertise
Paul Salvaggio	Connector Commodity Management	Interconnect Center of Expertise
Jan Cenedella	Cable Commodity Management	United States Distribution
Yvonne Pierce	DECwrite Files	Canadian Technology Center
Marcia Johnson	Illustration Scans	Electro/Mechanical Design and Support
AMP, Dupont, and Molex for use of their catalog illustrations.		

Chapter 6: Printed-Wiring Boards (PWB)

The Printed-Wiring Board (PWB) Electronics Technology File is a guideline of the technology necessary to design PWBs according to the latest available electronics and manufacturing processes. The chapter contains three types of information:

- Qualitative data for a design engineer to make trade-off decisions.
- Quantitative data about how certain design attributes perform.
- Explicit rules, along with the impact of deviating from the rules, are included in the Chapter 7, Module Layout Design Requirements.

6.1 Primary Printed-Wiring Board Features

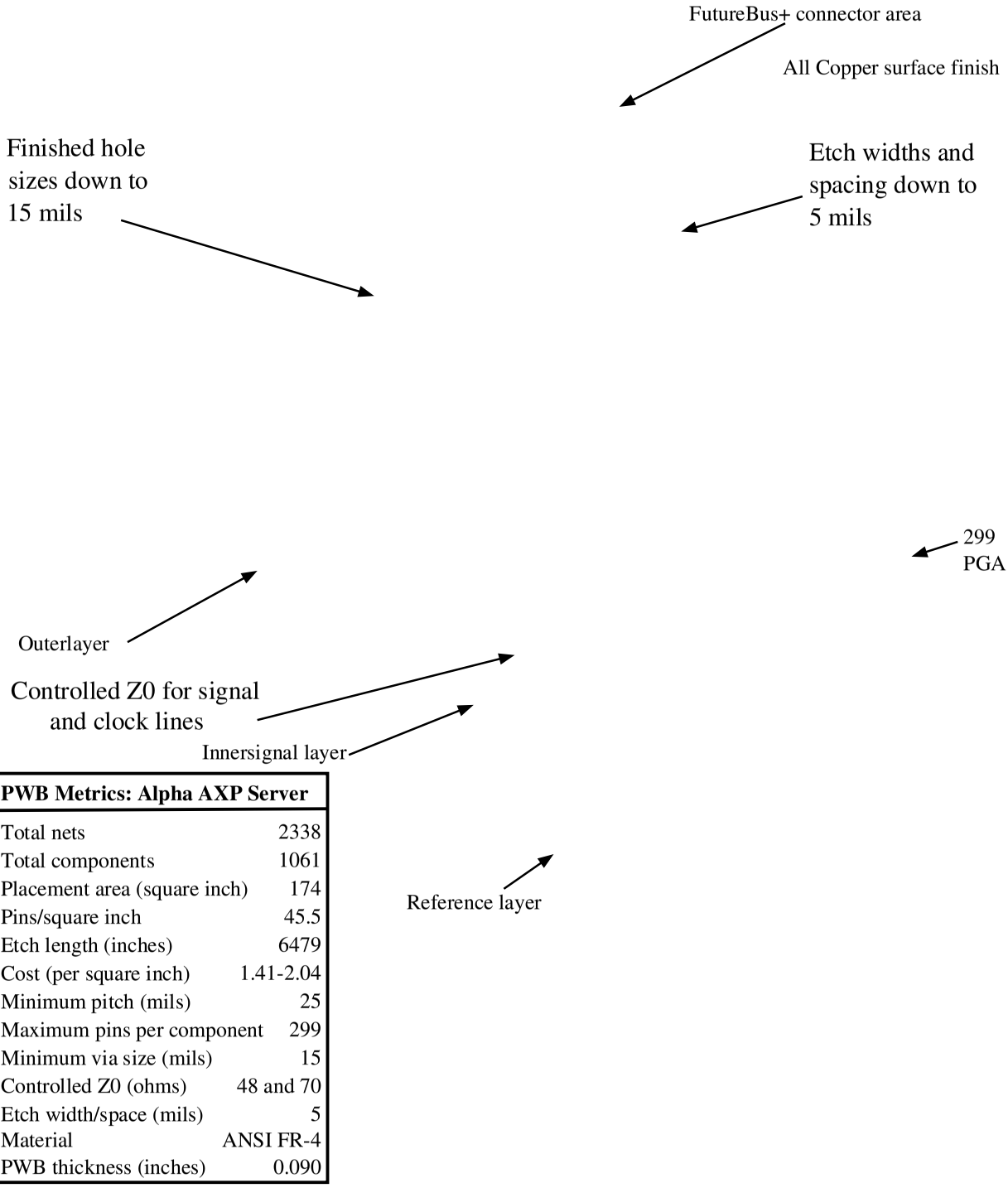
The following table displays the acceptable PWB attributes defining the outer limits of design from the Electronics Packaging Working Group (EPWG) strategy.

Attribute	Platform 3	Platform 4
Maximum circuit size (inches)	14 x 18	14 x 18
Minimum panel size (inches)	4.0 x 2.5	4.0 x 2.5
Minimum component lead pitch (inches)	0.020	0.50 mm
Maximum nominal board thickness (inches)	0.093	0.093
Dielectric constant @ 100 MHz	4.1	4.1
Number of layers (total)	8	12
Maximum number of routing layers (signal)	6	8
Minimum nominal finished hole size (inches)	0.012	0.010
Minimum through-hole pad (inches)	0.028	0.025
Maximum aspect ration (PWB Thickness/FHS)	8:1	10:1
Minimum nominal line width (inches)	0.005	0.004
Minimum nominal line space (inches)	0.005	0.005

6.2 Typical PWB Platform 3/4 Applications

The following examples demonstrate the breadth of potential applications that can be derived from the preferred and acceptable choices defined within this chapter. The examples demonstrate the PWB, Assembly, and Test rule compromises made by the concurrent engineering teams to achieve the overall product goals.

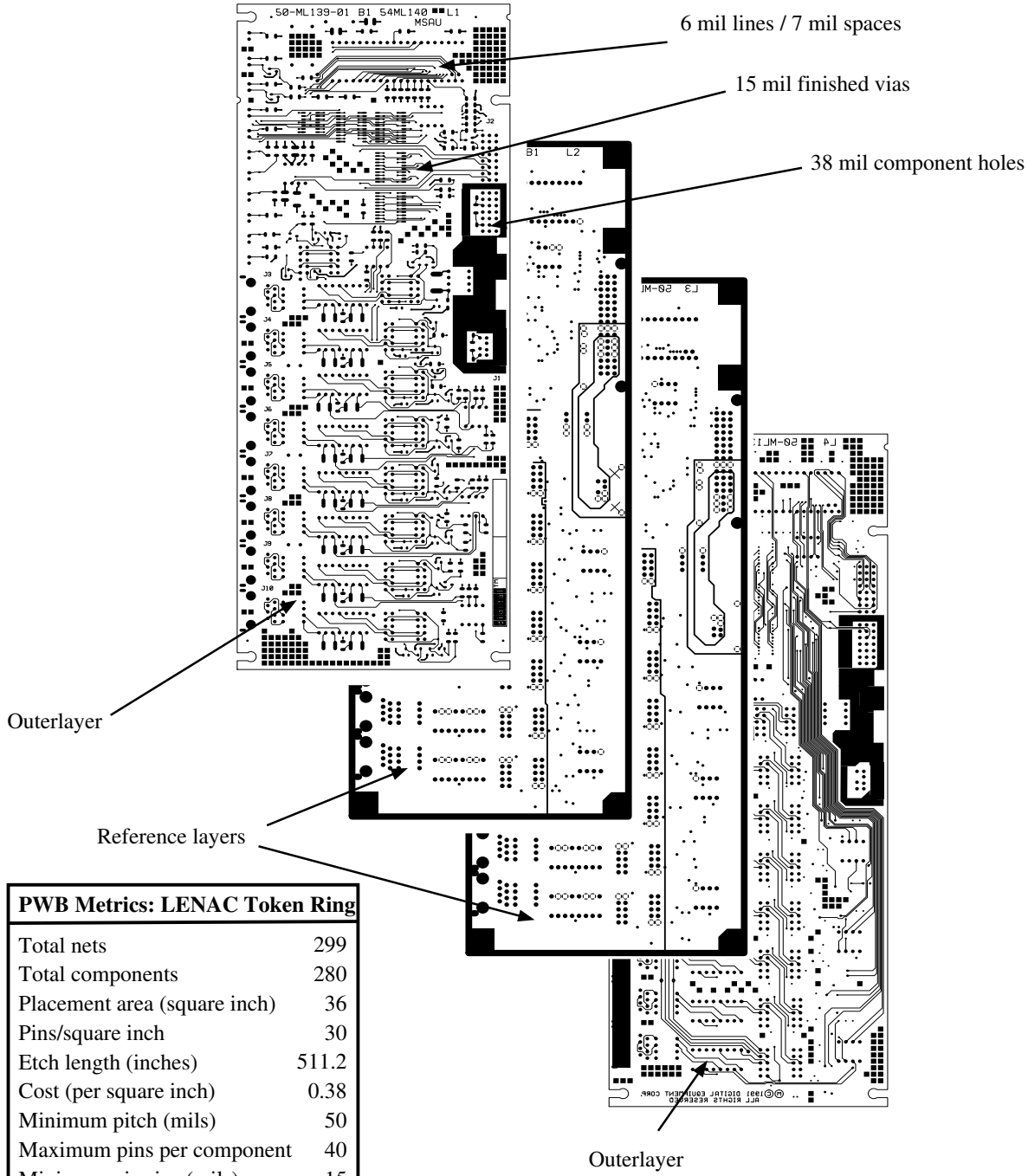
Driving Force	Example
Performance	Alpha AXP server
Cost	Token ring
Density	Low cost high density 2.5 inch disk controller.


FutureBus+ connector area
All Copper surface finish
Finished hole sizes down to 15 mils
Etch widths and spacing down to 5 mils
299 PGA
Outerlayer
Controlled Z0 for signal and clock lines
Innersignal layer
Reference layer

PWB Metrics: Alpha AXP Server	
Total nets	2338
Total components	1061
Placement area (square inch)	174
Pins/square inch	45.5
Etch length (inches)	6479
Cost (per square inch)	1.41-2.04
Minimum pitch (mils)	25
Maximum pins per component	299
Minimum via size (mils)	15
Controlled Z0 (ohms)	48 and 70
Etch width/space (mils)	5
Material	ANSI FR-4
PWB thickness (inches)	0.090

Figure 6-2: Cost-driven PWB Designs

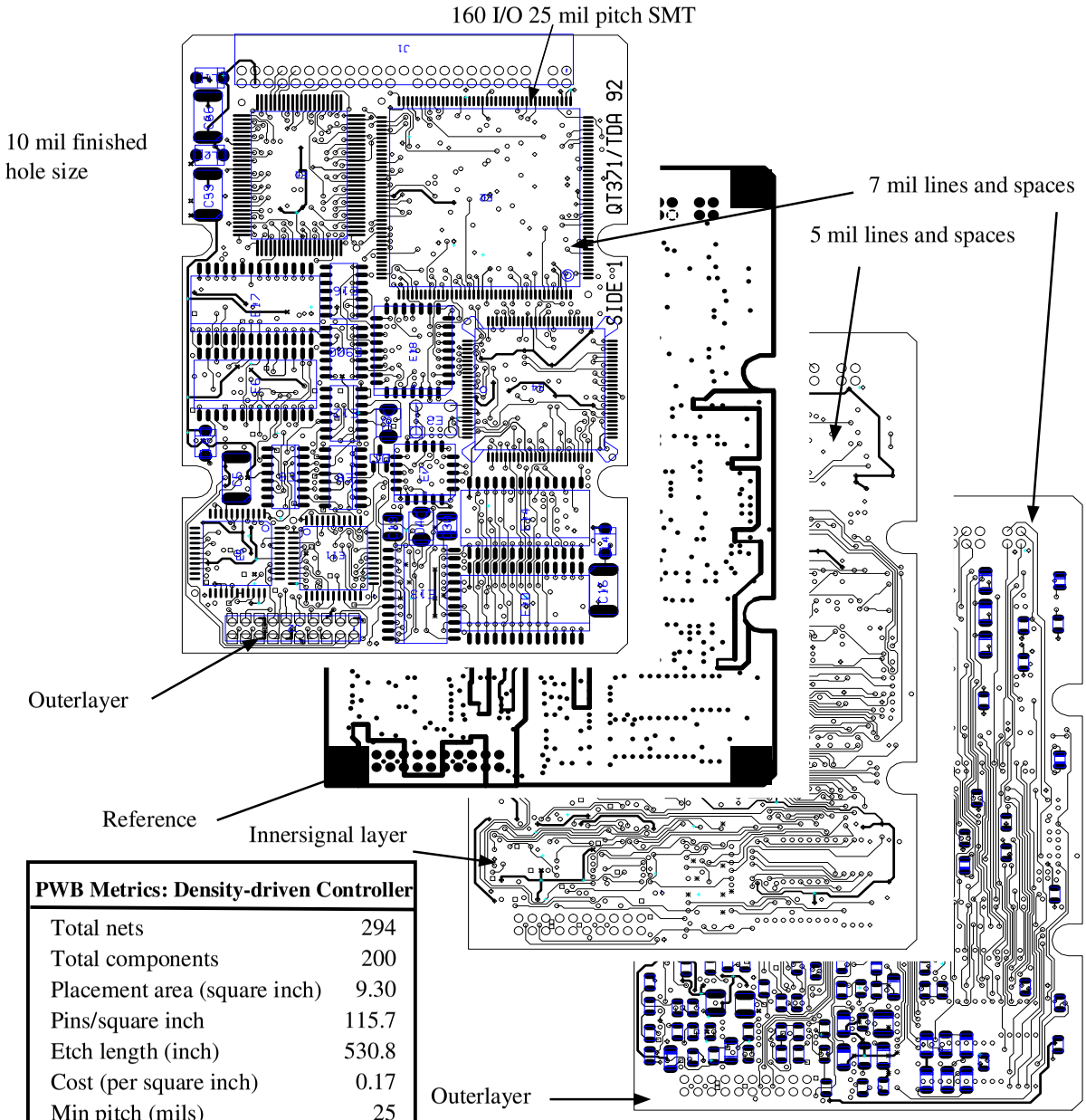
This figure of a LENAC token ring — 4 layer design shows how cost-driven considerations forced a potential six or eight layer PWB to four layers through extensive manual routing, minimal signal integrity rules and courser etch.



PWB Metrics: LENAC Token Ring	
Total nets	299
Total components	280
Placement area (square inch)	36
Pins/square inch	30
Etch length (inches)	511.2
Cost (per square inch)	0.38
Minimum pitch (mils)	50
Maximum pins per component	40
Minimum via size (mils)	15
Controlled Z0 (ohms)	None
Etch width/space (mils)	6/7
Material	ANSI FR-4
PWB thickness	0.062

Figure 6-3: Density-driven PWB Designs

This figure of a low-cost, high-density disk controller 2.5 inches disk drive — 4 layer design shows how low I/O devices can be placed for maximum density and minimal cost if the trade-offs are well understood between assembly DPU levels and a no repair/no in-circuit test strategy.



PWB Metrics: Density-driven Controller	
Total nets	294
Total components	200
Placement area (square inch)	9.30
Pins/square inch	115.7
Etch length (inch)	530.8
Cost (per square inch)	0.17
Min pitch (mils)	25
Max pins per component	160
Min via size (mils)	10
Controlled Z0 (ohms)	None
Etch width/space (mils)	7
Material	FR-4
PWB thickness (inches)	0.030

6.3 Printed-Wiring Board Preferred and Acceptable Attributes

The following sections detail preferred and acceptable attributes for PWBs.

6.1 Materials

Attribute	Preferred	Acceptable
Material	Difunctional FR-4	Multifunctional FR-4
Copper Minimal Nominal [Absolute Minimum after PWB Processing]		
Outerlayer foils	0.0007 min [0.0003]	0.0007 min [0.0003]
Copper Plating	0.0010 min	0.0010 min
Innersignal Layers	0.0014 min [0.0010]	0.0014 min [0.0010]
Innerlayer Reference	0.0014 min [0.0010]	0.0028 min [0.0022]

All dimension in inches.

Table 6-1: PWB Material Properties

FR-4 Material Properties (Difunctional)	
Dielectric Constant @100 MHz	4.1 ±10%
Dielectric Withstanding Voltage Minimum	750 Volts/mil
Dissipation Factor @100 MHz	0.21 - 0.24
Glass Transition Temperature Tg	115/125 °C
Coefficient of Thermal Expansion	
Z axis below Tg (ppm)	60
Z axis above Tg (ppm)	350

Copper and Solder Properties	
Cu Specific Resistance (μohm/mm)	1.712
Cu Coefficient of Linear Expansion (ppm/° C)	17.3
Solder Electrical Conductivity (% of Cu)	11.5
Copper Thickness Cost Impact ($/Square Inch/Cu Plane)	
2.8 mil /2 ounce reference planes	$0.012

Notes:

- PWBs with 10 layers or greater with aspect ratios greater than 5:1 require Class III copper foil which must be specified on the mechanical drawing . (Aspect Ratio is PWB Thickness/Finished Hole Size)
- MFFR-4 is recommended for high value-added assemblies with aggressive assembly and repair processes.
- Copper foil thicknesses are derived from ounces per square foot and copper density. One ounce = 0.0014 inch.

6.2 Surface Finishes

Attribute	Preferred	Acceptable
Surface Finish	Hot Air Solder Leveled (HASL)	Reflowed Tin/Lead (63%/37%) All Copper
Surface Finish Tolerance	Solder Surface 150 µin minimum at crest	N/A for All Copper
Gold/Nickel	30 µin minimum of Gold 100 µin minimum of Nickel	50 µin minimum of Gold 100 µin minimum of Nickel
Soldermask	Liquid Photoimageable	Screened (>10 mil line/space)
Liquid Photoimageable Soldermask		
Soldermask width nominal inches	≥0.008	≥0.006
Feature clearances nominal inches	≥0.0025	≥0.0015

Notes:

- HASL surface finish thicknesses may be less than 150 µin minimum at some locations on the circuit.
- The cost of liquid photoimageable soldermask is $0.008 per square inch per side. The cost of screened soldermask is $0.003 per square inch per side for >0.010 inch lines/space applications.
- Use all copper only when absolutely required. The all copper surface finish is **only** compatible with an organic acid/water clean assembly process. It is **not** compatible at present with a no-clean assembly process.
- Gold finishes are $0.40 per plated square inch.

6.3 Overall Dimensions

Attribute	Preferred	Acceptable
Maximum Finished Circuit Size	10.5 × 16	14 × 18
Finished Circuit Size Tolerance <18 inches Circuit Dimension	±0.015	±0.005 for (Route only) ±0.008 (Route, shear, V-groove)
Thickness Nominals	0.062	0.093
Thickness Tolerance	±10%	±10%
Surface Feature to Feature (TPD)	0.008 TPD[1]	0.006 TPD[2]

All dimensions in inches

[1] Currently available; need not be specified.
[2] Requires specification on mechanical drawing. Certain restrictions apply with respect to PWB supplier capability. Contact section owner.

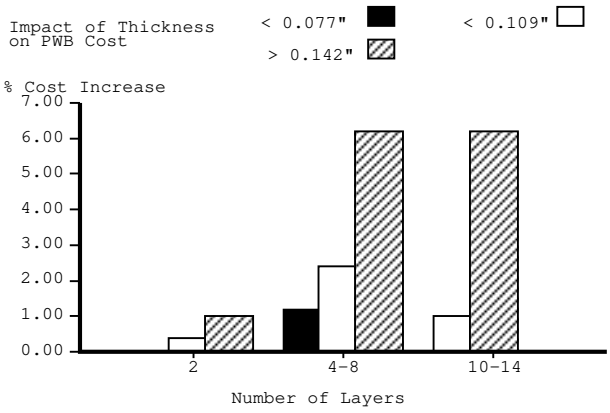
Notes:

- Maximum circuit size for **assembly processing** is 14 × 18 inches.
- Add 1% cost for ±0.005 inch circuit edge tolerance for NC router set-up and processing
- For slots, notches, and cut-outs, allow 0.040 inch minimum radius and ±0.005 inch tolerance if routed by PWB supplier
- There is a significant cost impact for through-hole components if PWBs over 0.093 inch nominal are required.
- Thicker PWBs are a cost premium. Increasing PWB thickness with additional prepreg or core material adds cost. PWBs greater than 10 layers are typically not less than 0.077 inches.

Table 6-2: Maximum PWB Warp (as received before assembly)

Nominal Thickness inch	mm	Maximum Warpage Ratio (deflection / span)
Less than 0.030	Less than 0.79	0.015
0.030-0.059	0.79-1.6	0.010
0.060-0.089	Over 1.6-2.39	0.007
0.090-0.250	Over 2.39-6.3	0.005

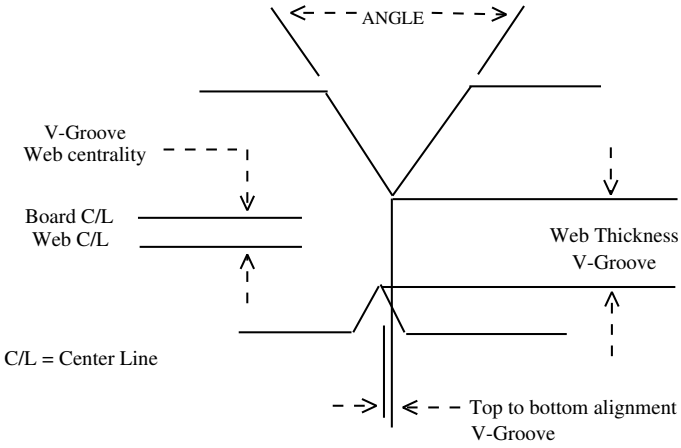
Graph 6-2: Impact of PWB Thickness on Cost



6.4 V-Grooving

V-Grooving, utilized when components must unavoidably overhang the edge of the finished circuit, entails removing material from both sides of a PWB thickness to provide a determined plane of separation as well as define the finished circuit edge.

Figure 6-4: V-Grooving in PWB



Limitations - based on current manufacturability data.

- 0.050 - 0.065 inch PWB thicknesses only
- Up to 6 layers maximum
- Up to 50 mil pitch SMT or greater
- Contact section owner when new product applications exceed the above

Requirements

- V-Groove angle: 60 ± 5° is preferred. Expanded range of 30°- 60° is acceptable but may limit PWB supply base.
- V-groove web thickness: 0.014 inch ±0.002 inch; no deviation
- V-groove web centrality: ± 0.007 inch; no deviation
- V-groove top-to-bottom alignment: ±0.004 inch; no deviation

6.5 Line widths and Spaces

Attribute	Preferred	Acceptable
Line widths and spaces		
Internal lines	≥0.006	≥0.005
Internal spaces to pad/line	≥0.0075	≥0.005
External lines	≥0.008	≥0.006
External spaces to pad/line	≥0.010	≥0.007

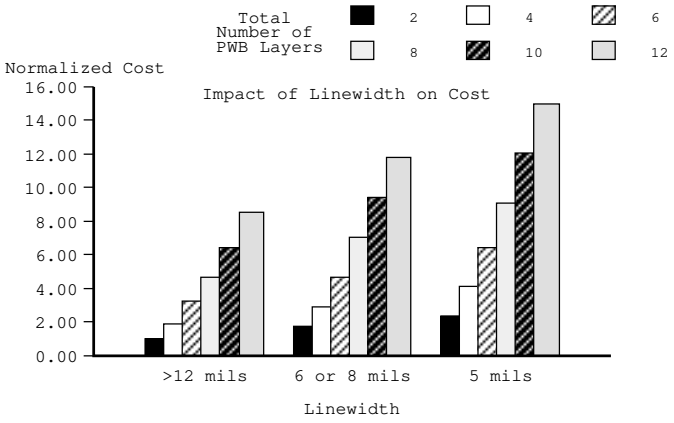
All dimensions in inches.

Table 6-3: Line width Tolerances

Line width Tolerance (inches)	
Nominal Width	Line Width Tolerance
0.005	±0.001
0.006	±0.002
0.008	±0.002
0.012	±0.003
0.015	±0.003
0.020	±0.003

Finer lines and spaces add cost. Trade-offs between line widths and spaces, layer count, and design constraints must be made to derive the lowest cost PWB.

Graph 6-3: Line width Cost



Notes:

- Designers need to be aware of the trade-offs between finer lines and more layers. Refer to **Graph 6-2**.
- For Controlled Impedance, do not specify BOTH impedance and line width tolerances, specify only impedance nominal and tolerance.
- Line widths are measured at the interface of the copper and dielectric material. The top of the conductor is typically reduced by two times the base foil thickness resulting in a trapezoidal shaped conductor cross section
- 5 mil outerlayer lines are feasible with a 10% - 15% cost adder.

6.6 Hole Size and Hole Density

Attribute	Preferred	Acceptable
Finished hole size	≥0.015	≥0.010
Finished Hole sizes	0.015, 0.020, 0.032, 0.038, 0.041, 0.042, 0.055, 0.059	0.010
Hole density average	<30 holes per square inch	<120 holes per square inch
Aspect ratio (PWB thickness to finished hole size)	<5:1	≤10:1

All dimensions in inches.

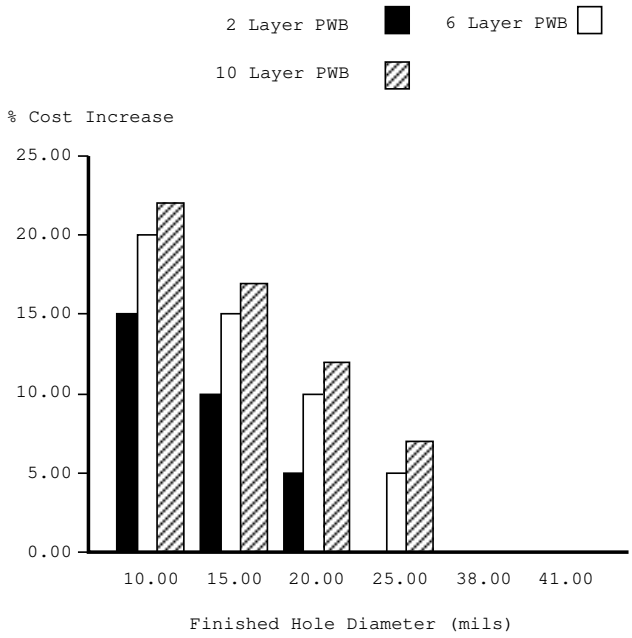
Table 6-4: PTH and nonPTH Diameters Tolerances

PTH and nonPTH Diameters and Tolerances

Nominal Diameter (Inches)	Tolerances (Inches)
Component Holes	
0.032	±0.003
0.034	±0.003
0.038	+0.004/-0.003
0.041	+0.002/-0.003
All Other Holes	
0.063 and under	±0.004
Over 0.063 - 0.250	±0.005
Non-PTH Hole Diameters	
Under 0.125	±0.003
0.125-0.250	±0.005
Over 0.250	±0.005
0.157 (Tooling)	±0.002

Graph 6-4: PTH Costs

Smaller finished hole sizes increase cost. Smaller drill sizes require higher grade drill machines, costlier drill bits, lower board stack height, slower feed rates, and longer drilling times.



Notes:

- Aspect ratios over 5:1 require longer plating times, resulting in increased costs.
- Minimize different hole size choices to reduce drill set-up times
- Hole densities of 30 holes per square inch are 4% to 8% of total PWB cost; increased via densities result in a commensurate increase in total cost.
- To achieve hole size tolerances requires the addition of autothieving.
- Drilled hole true position diameter is 0.0085 inches (±0.0030 inches)
- Tighter hole diameter and the position tolerances add cost (up to 5%); autothieving and outerlayer etch optimization are critical.

6.7 Lay-ups and Continuity Testing

Attribute	Preferred	Acceptable
Layers	2, 4, and 6	8, 10, and 12
Test Point Density	100 pins/square inch maximum	200 pins/square inch maximum

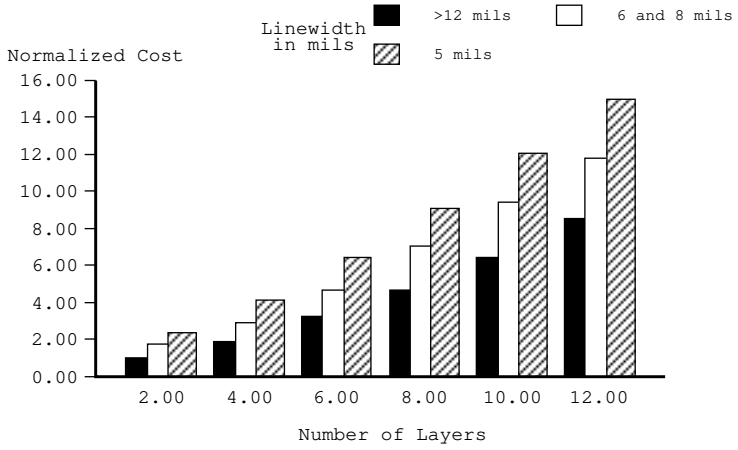
Commonly used laminate thicknesses are: 6, 7, 8, 10, 12, 14, 16, 18, and 20 mils thick. There are two commonly used laminate thickness tolerances: Class I and Class III. Class III is a 2 - 3% cost premium over Class I for the raw material. Classes are based on Mil-P-13949.

Table 6-5: Standard Laminate Thicknesses and Tolerances

Laminate Thickness (inches)	Class I	Class III
0.0046 - 0.0065	±0.0015	±0.0007
0.0066 - 0.0120	±0.0020	±0.0010
0.0121 - 0.0199	±0.0025	±0.0015
0.0200 - 0.0309	±0.0030	±0.0020
0.0310 - 0.0409	±0.0065	±0.0030

Increasing layer count adds cost. Trade-offs between line widths, spacing, layer count and design constraints must be made to derive the lowest cost PWB.

Graph 6-5: Impact of PWB Layer Count on Cost



Notes:

- Lay-ups should be of symmetric construction and should contain an even number of layers. Signal over reference plane construction is preferred on core laminates.
- **Bed-of-Nails** —Typical continuity test fixture cost is $0.20 - $0.25 per pin.
- **Clamshell Fixture** — Double-sided testing is required when network end points are located on both sides of the PWB. The cost can be up to $3.50 per pin.
- **Flying Probe Tester** — Point-to-point testing is 1,250 nets per hour at $75 per hour.
- Continuity testing can test component pitches down to 0.5mm.

6.4 Electrical Characteristics

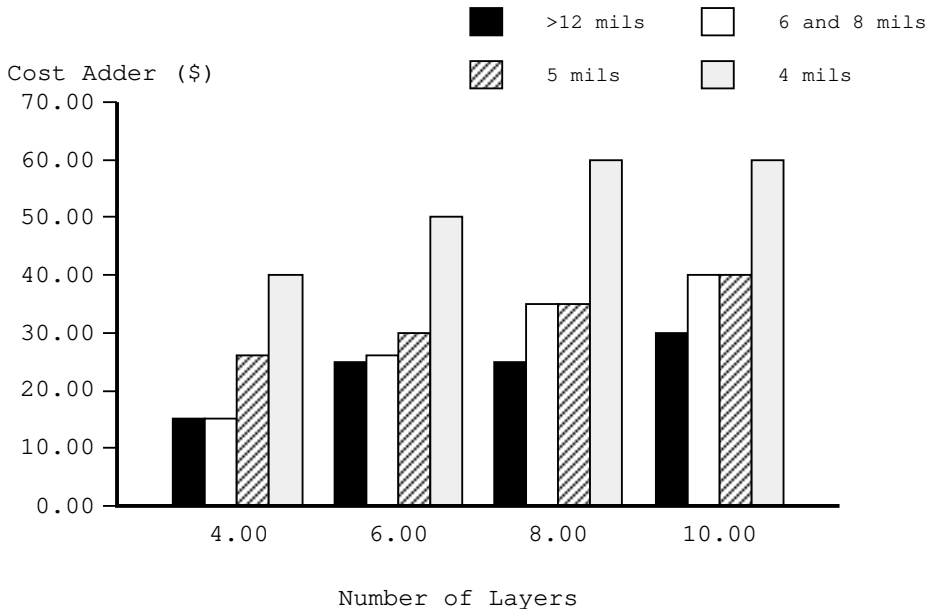
The following sections detail electrical characteristics of PWBs.

6.1 Controlled Impedance Tolerance

Attribute	Preferred	Acceptable
Microstrip (surface and embedded)	±20%	<20% - 15%
Stripline	±15%	<15% - 10%
Asymmetric stripline	±15%	<15% - 10%

Controlled impedance requirements add significant cost. The need for separate impedance coupons for each circuit, special impedance testing, recording data, serializing coupons, and shipping add $10 to $20 minimum per controlled impedance PWB.

Graph 6-6: Cost of Controlled Impedance



Notes:

- Designs that meet functional objectives with preferred controlled impedance tolerances should not be specified as controlled impedance designs.
- Preferred controlled impedance tolerances are achieved at no cost if qualified lay-ups are used.
- Acceptable impedance tolerances must be measured on a per circuit basis adding cost shown in **Graph 6-5**.

6.2 Controlled Impedance Testing - General

When a controlled impedance design is specified, manufacturing conformance is usually verified by measurement of a single etch on each impedance controlled layer. The preferred method is to use a selected functional etch; as an alternative, test etch, or coupon is provided inside the circuit area; the least desirable is to use a coupon outside the test area.

Notes:

- Use of in circuit etch or in circuit coupons, will reduce circuit cost $10.00 - $20.00 by alleviating requirements for coupon marking, test data compilation, tracking and shipping.

Costs are decreased through use of characterized lay-up kernels, and expanding impedance tolerance from ± 10% to ± 15%.

6.3 Characterized Lay-up Kernels

Table 6-6: Typical Lay-up Kernels

This is a sample table showing the lay-up kernels.

Lay-up Kernel Physical Description	Line width mils	Impedance Ω	Tpd ns/inch	Rdc mΩ/inch	Rac mΩ/sqrt (MHz) inch
---------- Reference 10.0 ± 1.5 mils	5	61.0 ± 11	0.1797 ± 0.004	99 +25/-16	31 ± 0.003
---------- Signal 14 ± 2.0 mils	8	52.6 ± 9	0.1797 ± 0.004	62 +9/-7	23 ± 0.001
---------- Signal 10.0 ± 1.5 mils ---------- Reference	11	45.8 ± 8	0.1797 ± 0.004	45 ± 4.5	18 ± 0.001
---------- Outerlayer Signal (L1) 8.0 ± 1.5 mils	13.5 (L1)	72.0 ± 11	0.1403 ± 0.005	34 ± 2.5	15 ± 0.001
---------- Signal (L2) 8.0 ± 1.5 mils ---------- Reference	5 (L2)	62.9 +8.2/10.4	0.1724 ± 0.006	99 +16/-12	28 ± 0.001

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Chapter 7: Module Layout Design Requirements

The purpose of this chapter is to define module layout design requirements that will result in a manufacturable module with the lowest module assembly and test added value cost. The chapter contains five major sections.

Section 7.1 is a listing of the layout rules contained in this chapter.

Section 7.2 is a Module Layout Checklist that highlights critical module design issues. It emphasizes those rules which enable manufacturability and those which improve quality and decrease cost. The checklist refers the design team to the specific rules concerning these issues.

Section 7.3 contains the module layout rules. It is understood that each module has unique requirements as far as customer needs, functionality, cost, quality and time-to-market goals. This is why the rules are presented not as standards that must be followed, but as recommendations for the least-cost manufacturing process, with information to allow the design team to explore alternatives and understand the impact of their decisions. Each design rule is presented in two or more parts. First is the design rule itself, which represents the **preferred** and **acceptable** design choices. If these rules are followed, the result is the least-cost, highest quality module assembly and test process. The next part details the impact of not following the rules to cost and quality. In many of the rules, the impact is followed by a set of manufacturable alternatives or solutions.

Section 7.4 contains Surface Mount Technology Footprint patterns. Each component style is described with a figure and a table which contains the footprint dimensions.

Section 7.5 contains Through-Hole Footprints patterns. Each component style is described with a figure and a table which contains the footprint dimensions.

Section 7.6 is the Technical Background section where information pertaining to the Module Assembly and Test processes can be found. This includes typical process flows, process element physical constraints, and tolerance analyses.

Contributions from the manufacturing plants and product representatives, as well as the core team have been significant and appreciated.

7.1 Module Layout Checklist

Many module design factors influence the assembly cost and quality of a module. The following is a quick checklist of important design factors which should be considered prior to component selection and module floor-planning. Section 7.2.1 describes those design factors which enable basic module manufacturability. Section 7.2.2 and Section 7.2.3 describe design choices which impact module quality and module test capability.

7.1.1 Design Factors That Enable Module Manufacturability

Making design choices which allow for the use of existing process equipment and tooling will result in the avoidance of development of new assembly tooling and/or process steps, both of which would add **significant** cost and impact the quality of the modules.

FOR ALL MODULES

Design Factor	Section	Rule
Module Shape	7.3.1	1-1
Tooling Holes/NPTH	7.3.2	2-1, 2-2, 2-4
Clearances	7.3.3	3-2
	7.3.4	4-1
Module Height	7.3.4	4-4
Soldermask	7.3.7	7-1, 7-2, 7-4, 7-5, 7-6
Interconnect/Etch	7.3.3	3-4, 3-5, 3-6, 3-11, 3-13, 3-14, 3-15
	7.3.9	9-1
Via Considerations	7.3.3	3-6, 3-8
Innerlayer Features	7.3.3	3-12, 3-13, 3-14
	7.3.8	8-1
Module Marking	7.3.6	6-1

FOR MODULES USING SURFACE MOUNT TECHNOLOGY

Design Factor	Section	Rule
Fiducials	7.3.2	2-5
Footprint Pattern	7.3.2	2-6
	7.4	
Etch	7.3.2	2-8
Component Clearance/Orientation	7.3.4	4-1,4-6
Vias	7.3.3	3-7, 3-8, 3-9, 3-10

FOR MODULES USING PLATED THROUGH-HOLE TECHNOLOGY

Design Factor	Section	Rule
PTH Finished Hole Sizes	7.3.2	2-1
PTH Footprint Pattern	7.3.2	2-7
	7.5	
Component Clearances/Placement	7.3.4	4-1
Heat relief pads	7.3.2	2-3
Vias	7.3.3	3-9, 3-10

7.1.2 Design Choices That Affect Module Cost and Quality

Making design choices which allow for the use of mature module assembly processes, the fewest assembly process steps, and a simple mix of component types and technologies will result in high quality, low cost modules.

Design Choice	Section	Rule
Components on side 2 of a mixed mount module	7.3.4	4-5
Component orientation for side 1 and side 2	7.3.4	4-2
Overhanging components	7.3.4	4-3
Barcode	7.3.6	6-4
Component numbering sequence	7.3.10	10-1
Use of Tantalum Capacitors	7.3.3	3-7
Etch	7.3.3	3-1, 3-3, 3-11
Module Marking	7.3.6	6-1, 6-2, 6-3
Soldermask	7.3.7	7-3

7.1.3 Factors to Consider When Planning to Use In-Circuit Test

There are several design decisions which impact the cost and feasibility of an in-circuit test.

Design Choice	Section	Rule
Test pad size, tolerance and accessibility	7.3.5	5-1
Vias		5-2
ICT hold-down pin clearance		5-3
Side 2 component height		5-4

7.2 Module Layout Rules

7.2.1 Module Outline

The following rules describe the outline of the Printed-Wiring Board (PWB)/Module. For maximum and minimum sizes, refer to **Chapter 6, Printed-Wiring Boards**.

Rule 1-1 Module Shape

Modules should be rectangular in shape without notches, protrusions, or rounded corners except when the product form-factor dictates otherwise. The module assembly and verification equipment and in-process conveyors are designed to handle rectangular shapes.

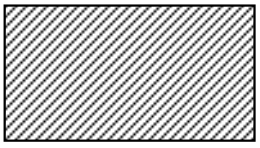
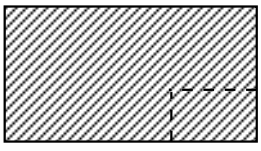
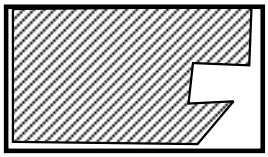
Impact:

A nonrectangular module shape results in poor panel utilization which:

- Increases cost due to excess scrap of PWB material (see Chapter 6, Printed-Wiring Boards), and may require an additional PWB material routing step that increases PWB cost by 1%.
- Requires that modules be made rectangular by either the use of break-away material or fixturing. See Figure 7-1.

Note: If inside corners are necessary, 0.04 inch minimum radius is required.

Figure 7-1: Alternatives for Achieving Rectangular Shapes

Alternative	Impact	Assembly Cost Impact ($)
Rectangular Module 	No additional costs required	0
Nothed Module with Break-away 	Additional labor cost required to remove prerouted break-away material after module assembly. **Note:** A V-groove or shearline needs to be continuous from panel edge to panel edge.	0.20 per module
Irregular shaped module with Assembly Fixtures 	Additional costs for assembly fixtures Additional labor cost for loading and unloading fixture Additional fixture maintenance cost Increased defect rate due to extra handling. See note above.	30,000 to 70,000 per product plus 0.50 to 1.00 per module

7.2.2 Feature Definition

The following rules should be used for the definition of features and feature sizes.

Rule 2-1 Hole and Pad Size Definition

Use common finished hole sizes (FHS) whenever possible and keep the number of hole sizes to a minimum. Refer to **Section 7.5** for common through-hole component PTH sizes and **Section 7.5.9** for calculating other PTH hole sizes.

Table 7-1 defines preferred and acceptable sizes for signal layer pads and clearance pads.

Table 7-1: Signal Pad/Clearance Pad Size Definition

Nominal FHS (inch)	Signal Pad Nominal (Inch)		Clearance Pad Minimum (inch)	
	Preferred	Acceptable	Preferred	Acceptable
0.010 Via	0.030	0.025	0.045	0.040
0.015 Via	0.035	0.030	0.050	0.045
0.020 Via/Soldered Component	0.040	0.035	0.055	0.050
0.028 FBus Press Pin	0.048	0.043	0.063	0.058
0.032 Via/Soldered Component	0.052	0.047	0.067	0.062
0.038 Via/Soldered Component	0.058	0.053	0.073	0.068
0.041 Press Pin	0.061	0.056	0.076	0.071
0.042 Soldered Component	0.062	0.057	0.077	0.072
0.055 Soldered Component	0.075	0.070	0.090	0.085
0.059 Soldered Component	0.079	0.074	0.094	0.089
0.067 Soldered Component	0.087	0.082	0.102	0.097
0.120 Soldered Hardware	0.145	0.140	0.160	0.155
0.157 Tooling Hole	none	none	0.192	0.187
0.250 Tooling Hole	none	none	0.285	0.280

If other hole sizes must be used, use the following equations to calculate pad sizes:

Preferred signal pad = FHS + 0.020 inch, Acceptable signal pads = FHS + 0.015 inch
Preferred clearance pads = FHS + 0.035 inch, Acceptable clearance pads = FHS + 0.030 inch

Impact:

- Multiple hole sizes increase PWB drill set up time and cost.
- Pad sizes are dimensioned to ensure acceptable alignment of drilled holes and inner and outer layer artwork in order meet PWB quality metrics.

Rule 2-2 Nonplated Through-Hole Criteria

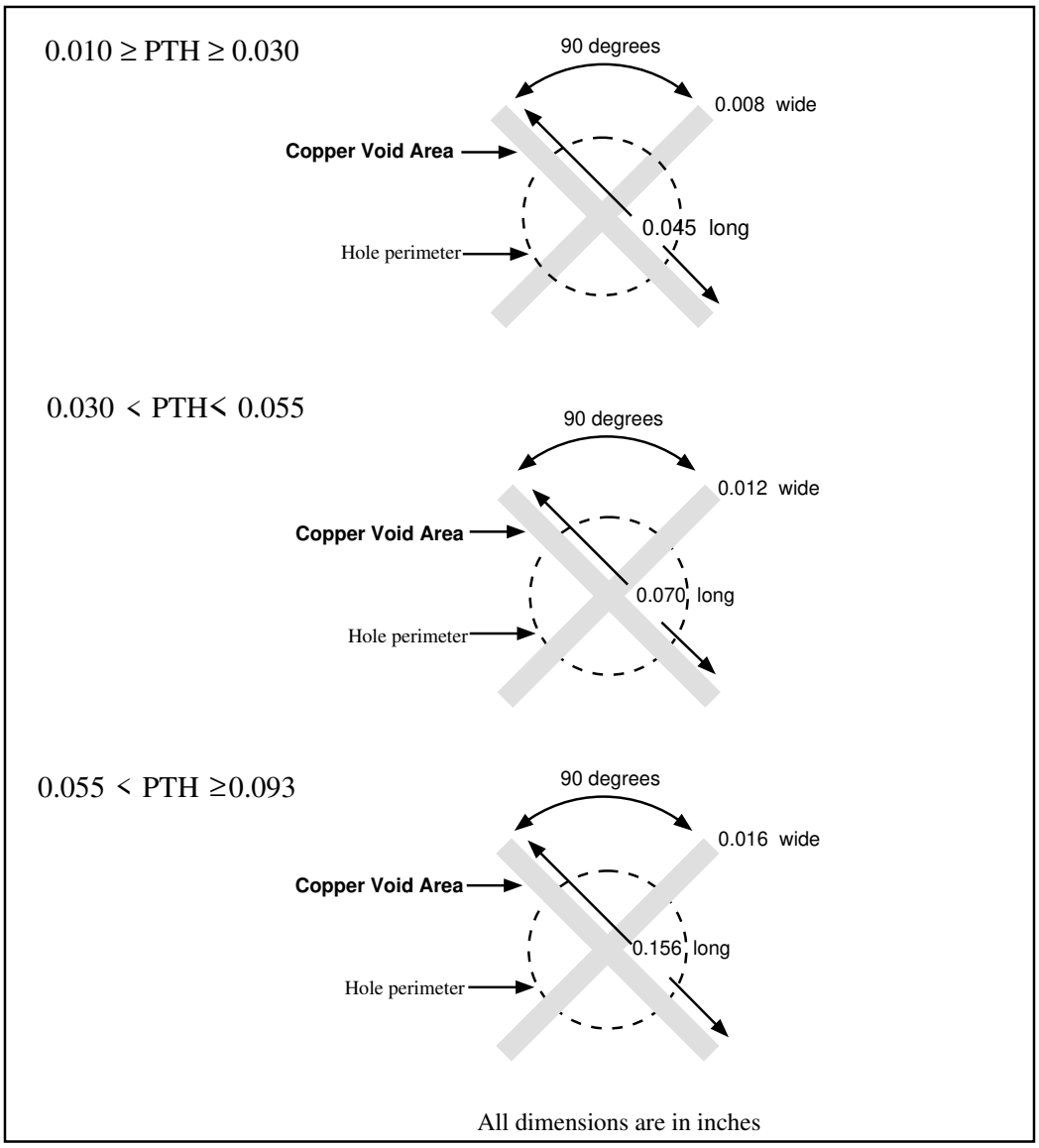
Design Requirements for nonplated through holes (NPTHs) are that NPTHs shall have no pads on outerlayers, innerlayer clearance pads on all innerlayers, and nominal diameters less than or equal to 0.250 inch

Impact: Nominal diameters greater than 0.250 inch require numerical control routing which adds 1% to the total cost of the PWB if no other routing steps are required.

Rule 2-3 Heat Relief Features

Heat reliefs must be used when a through hole component connects to a reference layer. The X-Shaped heat relief is the preferred choice, other shapes may cause inspection problems and confusion. Use the dimensions in Figure 7-2 to determine the size of the heat relief feature that is needed.

Figure 7-2: Heat Relief Dimensions



Impact:

- Too large a heat relief (copper void area) causes poor power or ground connections.
- Too small a heat relief causes the through-hole component to solder poorly and adds difficulty to the repair process.

Rule 2-4 Tooling Holes

Tooling holes are **nonplated** through-holes that are required to position modules accurately during the assembly and in-circuit test processes. Preferably, tooling holes should be within the module outline and should not be used for other purposes such as mounting handles. See Table 7-2 for tooling hole requirements and Figure 7-3 for design alternatives.

Table 7-2: Nonplated Tooling Hole Requirements

Tooling Hole Feature	Requirements
Quantity	4 (preferred) 3 minimum
Diameter	0.157 ± 0.002 inch
Clearance Area around tooling hole on side 1 and side 2	0.125 inch
Location	In each corner (See Figure 7-4 and 7-5)

Impact:

- **Nonpresence** - Absence of tooling holes produces an inability to accurately position modules throughout the assembly and test processes. In-Circuit Test (ICT) may not be feasible, and therefore the test cost per module increases 4 to 7% due to defects being found later in the verification process.
- **Diameter** - Manufacturing has standardized on 0.157 inch from edge; other sizes require new tooling.
- **Location** - Manufacturing equipment is standardized at 0.200 inch from edge; other dimensions require retooling.

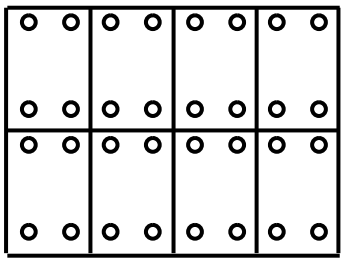
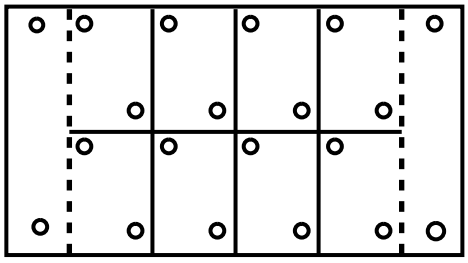
  Less than 0.200 inch from an edge or notch results in stresses in the tooling hole wall that can cause cracking of PWB material and the inability to V-groove.

  If tooling holes are not positioned in diagonal corners, ICT fixture contact reliability is decreased. Decreased contact leads to an increase in false failures and a 10 to 15% increase in test cost per module.
- **Clearance** - Is required by ICT fixturing.
- **Multiple Use -** ICT is often required after the final hardware, such as handles, is attached.

  ICT uses the tooling holes to locate test points. Obstructing hardware may have to be removed from tooling holes with a drill that can degrade the hole accuracy and may make ICT unfeasible.

Note: For V-groove panels, tooling holes need to be a minimum of 4 inches apart.

Figure 7-3: Module Tooling Hole Alternatives

Alternative	Impact	Preference
Tooling Holes Within Circuit Outline	No additional assembly costs No additional PWB material costs	Preferred Alternative
Tooling Holes On Tooling Strips	Added module assembly shearing or snap-off operation Additional PWB material cost No post-shear in-circuit test capability	Acceptable Alternative
Small Modules Multi-Up On Panel With Tooling Holes Within Circuit 	No additional assembly costs No additional PWB material costs	Preferred Alternative
Small Modules Multi-Up On Panel With Tooling Holes On Panel 	No Shearing capability, prerouted break-aways required Additional module assembly Snap-Off operation In-circuit test is feasible with two holes in diagonal corners of circuits	Acceptable Alternative

Note: If there are less than 2 tooling holes within the circuit, no post-separation in-circuit test capability exists.

Figure 7-4: Circuit Level Fiducial and Tooling Hole Placement for Standard Modules

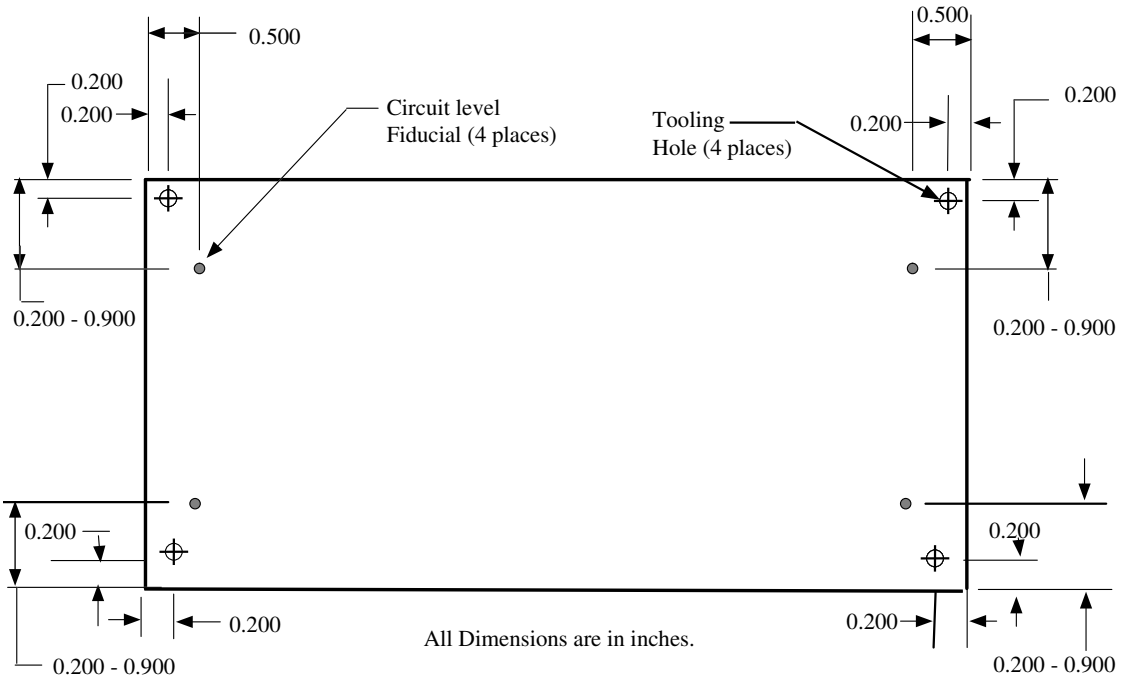
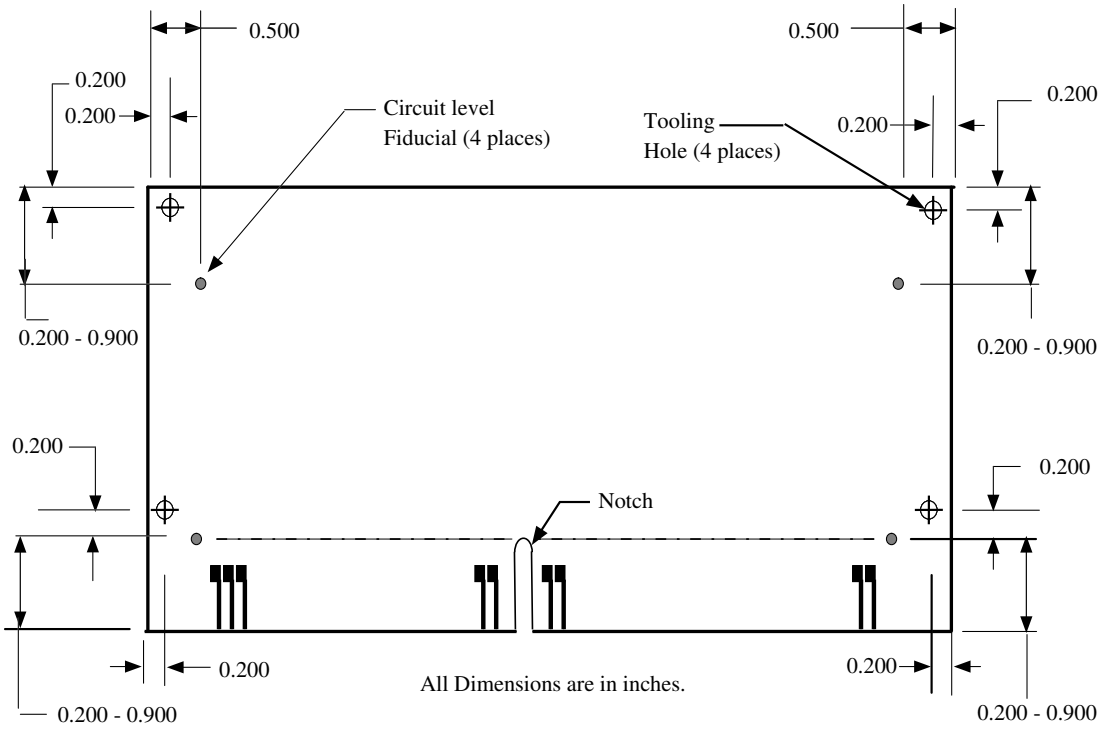


Figure 7-5: Circuit Level Fiducial and Tooling Holes Placement for Edge Card Module



Rule 2-5 Fiducials

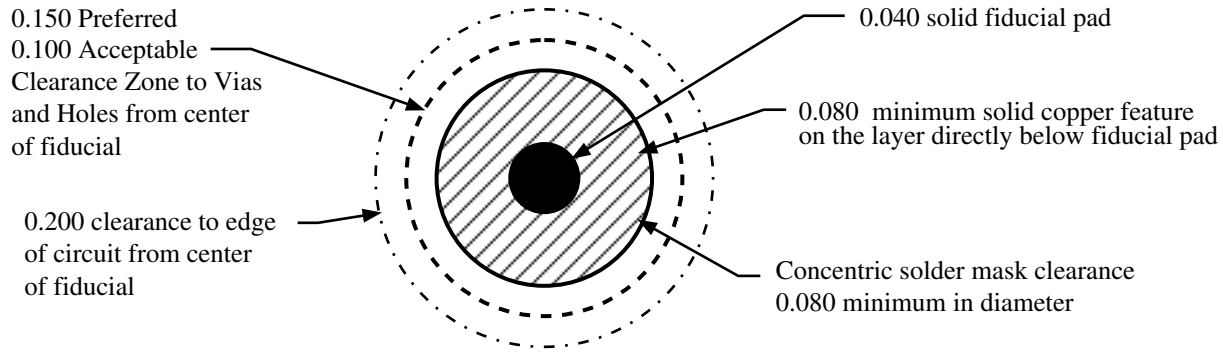
A fiducial is a feature found on the outer layer of the PWB that is **required** for vision-assisted circuit and component alignment during the surface mount process. Two types of fiducials are **required:**

- **Component level** fiducials are used to locate individual components during the placement process. They are required for 50 mil (0.050 inch) pitch components with 44 pins or more and for all components with less than 50 mil pitch. Component level fiducials are described as part of the footprint data.
- **Circuit level** fiducials are used to locate module surface features during the solder deposition and component placement processes. Two fiducials are used for each process step. Circuit level fiducials are required on both sides of the PWB if there are surface mount components on both sides.

Use the information in Table 7-3 to design fiducials onto a module. Fiducial locations are detailed in **Section 7.4** Surface Mount Footprints.

Table 7-3: Fiducial Design Requirements

Feature	Component Level Fiducial	Circuit Level Fiducial
Shape	Round	Round
Quantity	2	4
Location	See Section 7.4 SMT Footprints	Each corner (See Figure 7-4 & 7-5)



All dimensions are in inches and represent the measurement of concentric circles.

Impact:

The impact of not having fiducials increases misregistration of solder paste and components, resulting in increased defect levels and increased repair costs.

Alternatives:

For small modules that are processed (PWB and Assembly) multi-up on a panel, the circuit level fiducial requirements may be applied to the panel and not to the individual circuits.

For density-driven modules, where recommended component level fiducial locations are not possible, fiducials may be placed within the footprint such that the distance between them is 75% of the footprint pad pattern span. Fiducials may also be shared between adjoining components. See plant component placement experts for specific allowable locations. These alternatives lower the rotational accuracy of the placement.

Rule 2-6 Surface Mount Footprints

Use the surface mount footprint and pad designs for the specified component types found in **Section 7.4**. These footprint and pad designs are based on Digital component general specifications. The Techfiles account contains a directory of detailed footprint dimensions; refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

Impact:

Footprint and pad designs that are different than those specified in this document increase module assembly costs because the footprint and pad designs take solder joint geometry, component dimensions and tolerances, PWB feature tolerance, and placement equipment accuracy and tolerance into consideration. All of these dimensions and tolerances are critical to consistent, high quality, low cost placement of surface mount devices.

Rule 2-7 Through-hole Footprints

Use the through-hole footprint patterns in **Section 7.5**. This section details hole size, mounting centers, and hole patterns for common through-hole components.

Impact:

- If the hole is too large, the joint will not solder correctly.
- If the hole is too small, the holes, leads, or both, will be damaged during machine insertion. Hand insertion may be required as an additional process step. Minimum hole size for hand insertion is specified in Section 7.5.

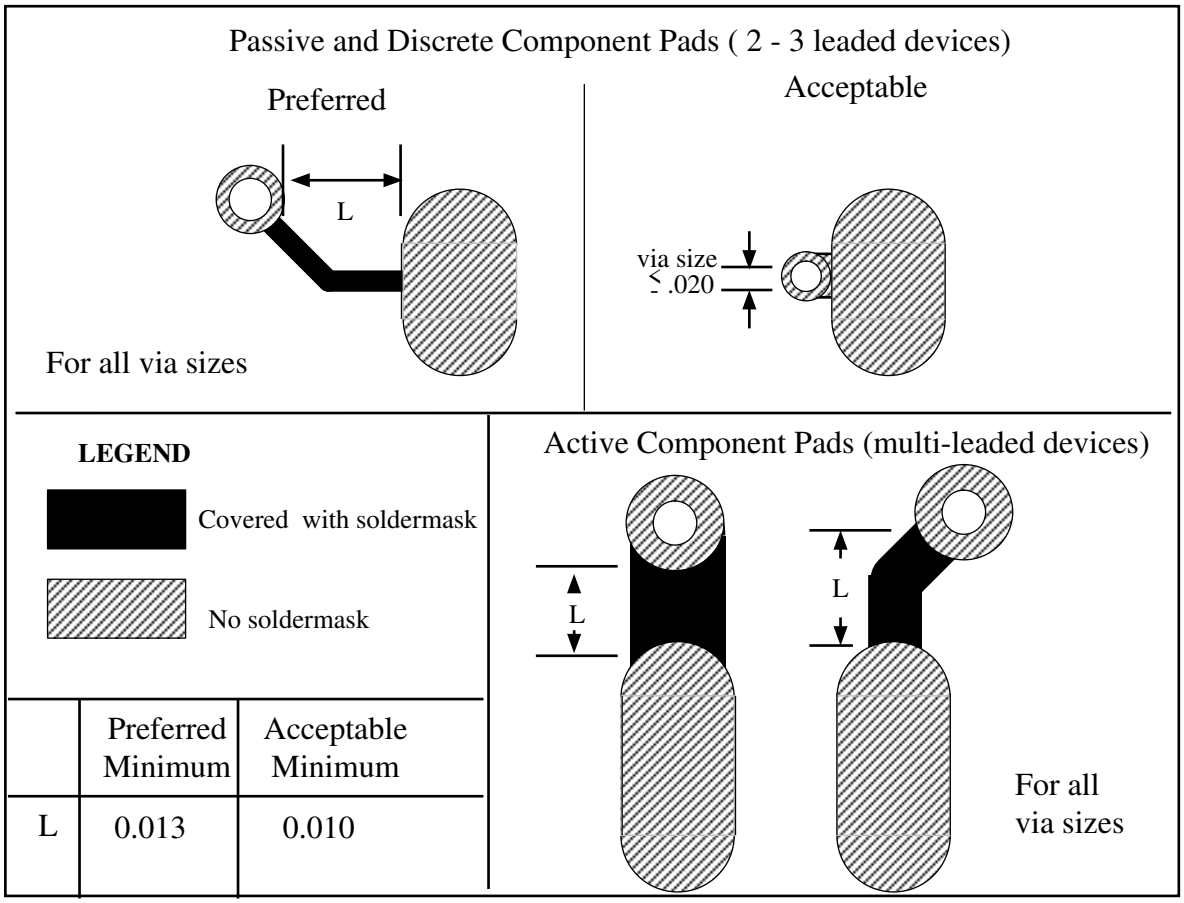
Rule 2-8 Dispersion Etch

Dispersion etch is required for all SMT component footprints. See Figure 7-6 for preferred and acceptable designs.

Notes:

1. For components that do not allow etch underneath, disperse out. (0805,1206,1210 body sizes)
2. For ferrite bead or inductor, dispersion etch should be wide.
3. Wide dispersion etch covered with soldermask is typically used for power and ground connections.
4. Acceptable cases do not necessarily provide a test via pad for ICT. When these technologies are used, dedicated test pads must be provided.

Figure 7-6: Dispersion Etch Configuration



	Preferred Minimum	Acceptable Minimum
L	0.013	0.010

Impact:

Use of other configurations result in insufficient solder joint defects.

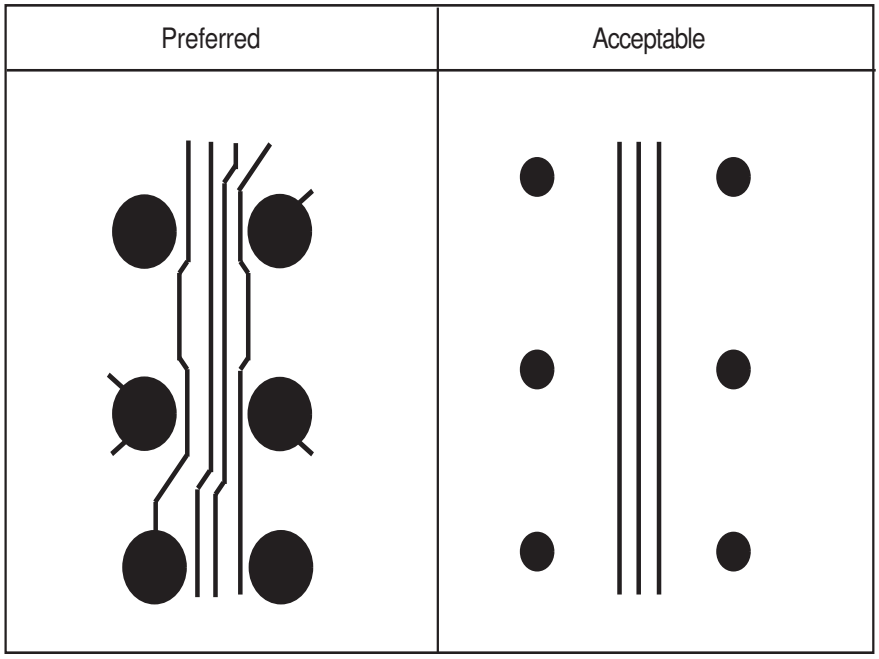
7.2.3 Etch Implementation

The following rules should be taken into consideration during the routing of the PWB/Module. For preferred line width dimensions, refer to **Chapter 6, Printed-Wiring Boards.**

Rule 3-1 External Conductor Spacing Optimization

Equalize conductor spacing pattern on external layers whenever possible. See Figure 7-7.

Figure 7-7: External Conductor Spacing Optimization



Impact:

Wider conductor spacing with thieving minimizes defects due to copper and solder overplating during the PWB manufacturing process. Also See **Rule 9-1,** Thieving.

Note: This rule is based on the limited capability of CAD systems to spread lines to achieve conductor spacing symmetry

Rule 3-2 Feature to Board Edge or NPTH Requirements

The following clearances to board edge and NPTH are required on all layers of multilayer boards. See Table 7-4.

Table 7-4: Feature to board Edge or NPTH Requirements

Feature to Circuit Edge	Minimum Distance (inch)
Component Pad	0.200
Nonfunctional feature	0.025
Functional Feature	0.050
Nonfunctional Feature to V-groove	0.050
Inner Signal Line	0.050
Vias Pad edge	0.100
Reference Planes	0.050
NPTH Perimeter	0.050
Test Point Center	0.125
Feature to NPTH	
NPTH	≥ PWB Thickness
Conductor	0.020

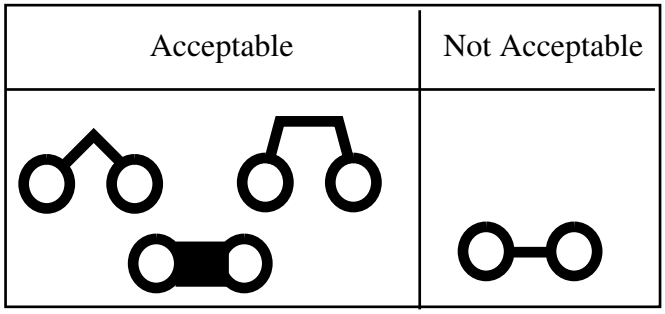
Impact:

- Adherence to these rules minimizes shorts during PWB fabrication and between the PWB and the system chassis, and are absolutely required for V-grooving.
- If NPTH is too close to the edge of the PWB or another NPTH, the hole wall material is prone to cracking.

Rule 3-3 Interconnections Between Adjacent Pads

For interconnections on **external** layers where pad-to-pad spacing is less than or equal to 0.045 inch, the etch must be angled or widened. See Figure 7-8.

Figure 7-8: Interconnections Between Adjacent Pads



Impact:

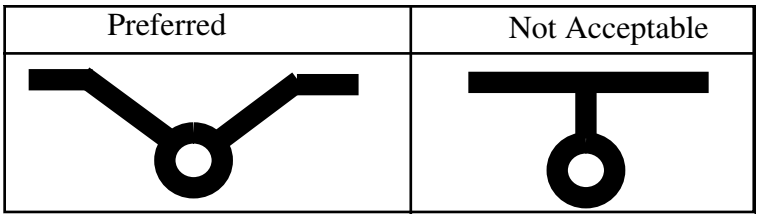
Angling or widening the etch reduces inspection problems because it is not mistaken for a pad-to-pad short.

Rule 3-4 Interconnections Between Pads and Lines

Apply the following to all line and pad interconnections:

- Lines must pass through the center of a pad.
- Lines must exit pad, perpendicular to the arc of the pad.
- Spacing from the edge of a pad to a bend point shall be 0.010 inch minimum.
- Connections between component pads and a passing conductor must be a minimum of 0.050 inch.
- Angles less than or equal to 90 degrees are not acceptable. See Figure 7-9.

Figure 7-9: Interconnection between pads and lines



Impact:

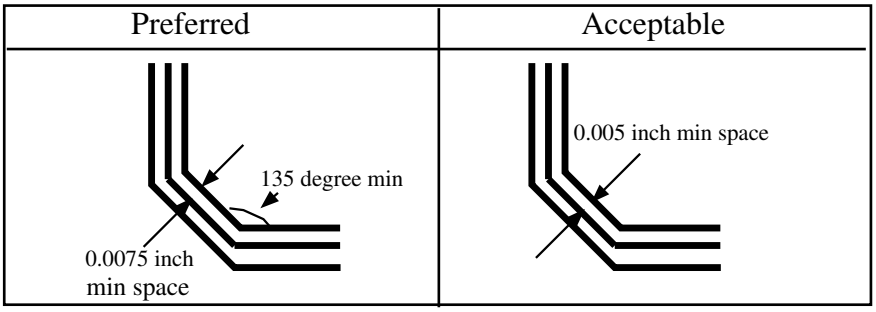
- The use of the recommended interconnections improves etching and soldermask coverage during PWB manufacturing.
- If interconnection rules are not followed, pad expansion cannot be done.

Rule 3-5 Conductor Bends

The preferred bend for all conductors is 135 degrees minimum. Rounded bends are allowed if spacing minimums between conductors are maintained. See Figure 7-10.

Note:
Use spacing minimums specified or smallest spacing on PWB whichever is greater.

Figure 7-10: Conductor Bends



Impact:

Using the preferred bend angles and conductor spacing improves etching and soldermask coverage during PWB manufacturing.

Rule 3-6 Vias Under Metal or Polystyrene Components

Vias are not allowed under metal or polystyrene components when the component body is less than 0.050 inch above the surface of the PWB. The recommend via pad edge to component body spacing is 0.050 inch.

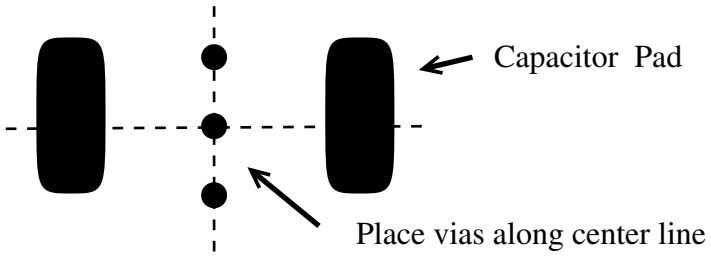
Impact:

If the via pad edge to component body is less than 0.050 inch, vias may short to components during reflow operation.

Rule 3-7 Vias Under Surface Mounted Tantalum Capacitors

Vias under surface mounted tantalum capacitors should be placed in the center of footprint pad pattern. See Figure 7-11.

Figure 7-11: Vias under Tantalum Capacitors



Impact:

If vias are too close to the termination pads, there is a potential to cause a short.

Rule 3-8 Via Restrictions

Vias are not allowed between the footprint pads of 0805, 1206 or 1210 packages, crystals, under screw-heads, or rivet heads that sit flat on the PWB.

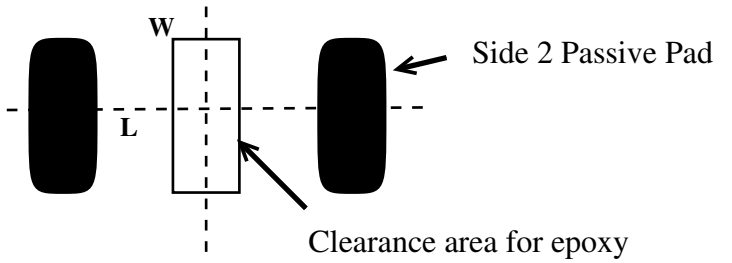
Impact:

There is a possibility of shorting due to the low profile of these component types.

Rule 3-9 Via Restrictions for Wave Soldered Modules

Vias are not allowed under the center of side 2 discrete components on a wave soldered module that is to be epoxied. See Figure 7-12.

Figure 7-12: Vias Under Side 2 Passives



	W (inch)	L (inch)
SMT Chip Components	0.040	0.090
SMT Tantalum Capacitors	0.080	0.170

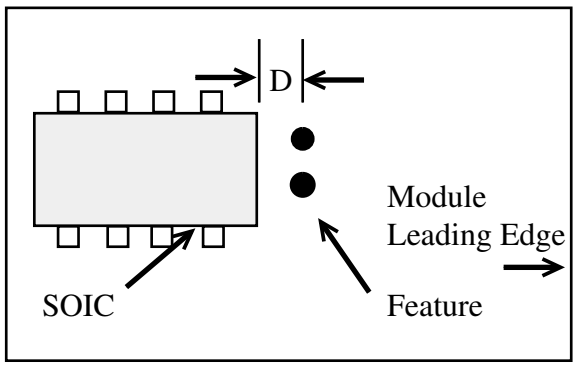
Impact:

If wave soldering is used for side 2 SMT discrete components, the epoxy may leach down the via and the device will not adhere resulting in reduced yield.

Rule 3-10 Via Restrictions for Small Outline Integrated Circuits (SOICs) on Wave Soldered Modules

Vias in front of SOICs on side 2 of wave soldered modules should be spaced. See Figure 7-13.

Figure 7-13: Vias in Front of Side 2 SOIC



Recommended Spacing from S2 SOIC Component Body	
Feature	D (inch)
Via	0.040
Component PTH	0.070

Impact:

The SOIC component creates a dam during the solder wave process and if vias are too close, solder bubbles through the PWB onto component body size.

Rule 3-11 Etch Restrictions

- Etch under 0805, 1206, and 1210 packages should be centered between pads.
- Surface etch connections for stake pins must be made on side 2 for pins installed on side 1, and on side 1 for pins installed on side 2.

Impact:

There is a possibility of shorting wires or components because the soldermask is not an adequate insulator between the PWB surface and wires.

Rule 3-12 Nonfunctional or Unused Innerlayer Pads

Nonfunctional or unused innerlayer pads for vias and plated through-holes should be supplied in the design data for every layer of the PWB.

Impact:

Standard practice within Digital is to supply unused pads with designs which aid in inspection and allows more predictable drilling during the PWB manufacturing process.

Rule 3-13 Venting of Large Open Areas in Innerlayer Copper Planes

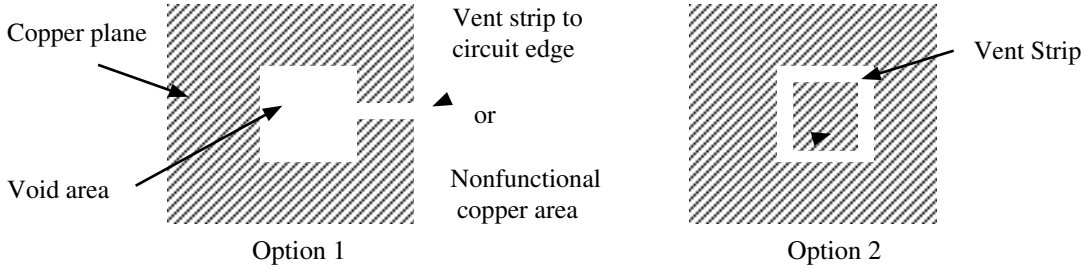
For openings in copper planes larger than 0.0625 square inches or 0.250 inch x 0.250 inch, one of the following two options must be applied:

1. Vent the opening in the copper plane to the nearest circuit edge. See Figure 7-14.

Innerlayer Copper Thickness	Vent Strip Width
1 ounce	0.031 inch
2 ounce	0.062 inch

2. Place an area of nonfunctional copper within the opening in the copper plane. The perimeter should have a clearance of 0.020 inch minimum.

Figure 7-14: Large Area Venting



Impact:

Volatile gas entrapment and delamination during PWB and assembly processing can occur if venting is not provided.

Note: Be aware that signal integrity of sensitive signal lines passing over interrupted reference planes can be adversely affected. Signal lines passing over nonfunctional copper areas are even more adversely affected.

Rule 3-14 Public Communication Carrier, AC Power and High Voltage Etch

Consult your local regulatory expert when designing telephone, power, and high voltage etch. Different countries have varying and continuously changing requirements.

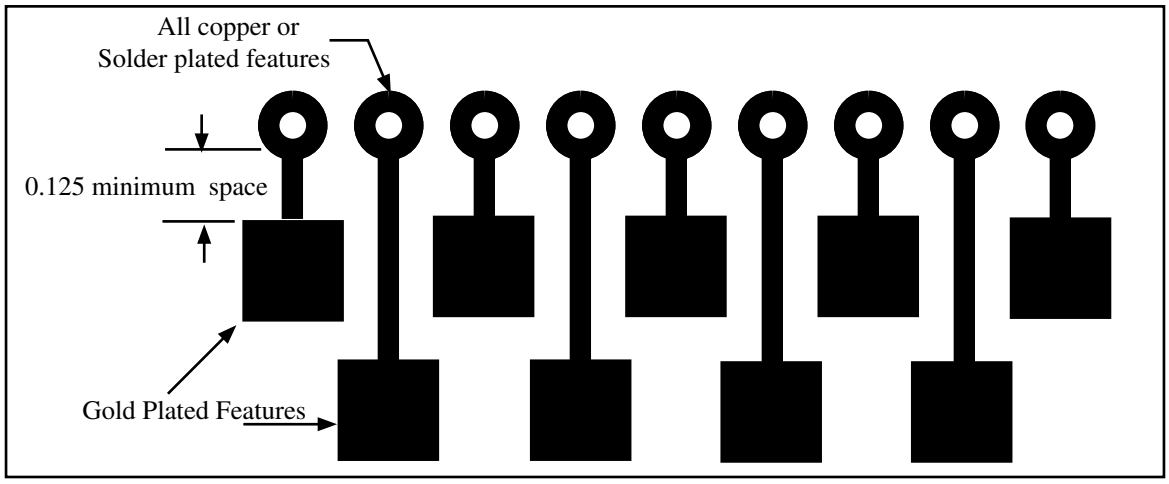
Impact:

There are specific rules that must be applied to ensure safe products and meet legally mandated requirements.

Rule 3-15 Gold Plating Spacing to Nongold Feature

- The use of gold plating is not preferred, but gold is necessary for card edge connectors. When gold plating is used, the minimum spacing allowed between the edge of a gold plated feature to the edge of a non-gold feature is 0.125 inch. Preferred clearance between gold plated features and component pads is 0.250 inch. See Figure 7-15.
- Gold plating features must be on the edge of a PWB, not within the center of a circuit area.
- Avoid placing conductors or other features in an area of the PWB that is to be gold plated.

Figure 7-15: Gold Plating Spacing to Nongold Features



Impact:

- Requirements tighter than 0.125 inch require special processing, resulting in an increased cost of 2 to 5% per circuit.
- Gold plating away from the edge of the PWB requires similar special processing.
- If components are placed too close to the gold finger area the following can occur:
  - Leaching of PWB chemistries causes opens in the PWB.
  - Transfer of solder paste onto finger area can occur.
  - Inadequate shielding space for side 2 wave solder process.

7.2.4 Component Placement

The following rules should be used during floor planning and layout of the module.

Rule 4-1 Component Clearance Requirements

The component and edge clearances which are shown in Figures 7-16 through 7-18 illustrate the clearances required by the Standard Assembly and Test Process. These clearances are typically driven by the inspection and repair processes. Detailed process element constraints can be found in **Section 7.6.2.**

SMT component dimensions are measured from **footprint pad** to **footprint pad** unless otherwise specified.

Through-hole component dimensions are pin center to pin center on the pin side, and body-to-body or body-to-pad as specified.

The clearances shown in Figures 17 and 18 for through-hole components assume a PTH hole size of less than 0.050 inch. See **Section 7.6.3**.

The spacing between two dissimilar components should be the larger of the two clearances specified.

Impact:

- If edge clearances are not provided, assembly fixtures are required which result in the following costs.

  Typical fixtures cost between $300 to $700 each; a product could require up to 100 fixtures depending upon volume, and the number of assembly plants. Additional process resources are required to load and unload fixtures at $0.50 to $1.00; additional handling increases opportunities for defects.

- Nonconformance to Component Clearance guidelines results in:

  Inability to assemble, inspect and repair components or test module.

  The need to remove adjacent components to repair defective components.

  The need for custom fixtures and nozzles for assembly or repair using the selective wave process. Nozzle fabrication costs increase by 25 to 50% for custom designs.

Alternatives:

For small circuits processed multi-up, apply edge clearance rules to the panel.

Bit Guard 0.15 μF capacitors may be mounted under SOJ DRAMS **ON MEMORY MODULES ONLY**. The Bit Guard capacitor is a 1210 package style that uses a standard footprint. It is 0.018 inch maximum height and is designed for surface mounting under DRAM SOJ packages. Testing on memory modules has shown the soldered capacitor required 0.021 inch maximum height and DRAM SOJs are specified with 0.025 inch minimum space.

Figure 7-16: Surface Mount Component Clearances

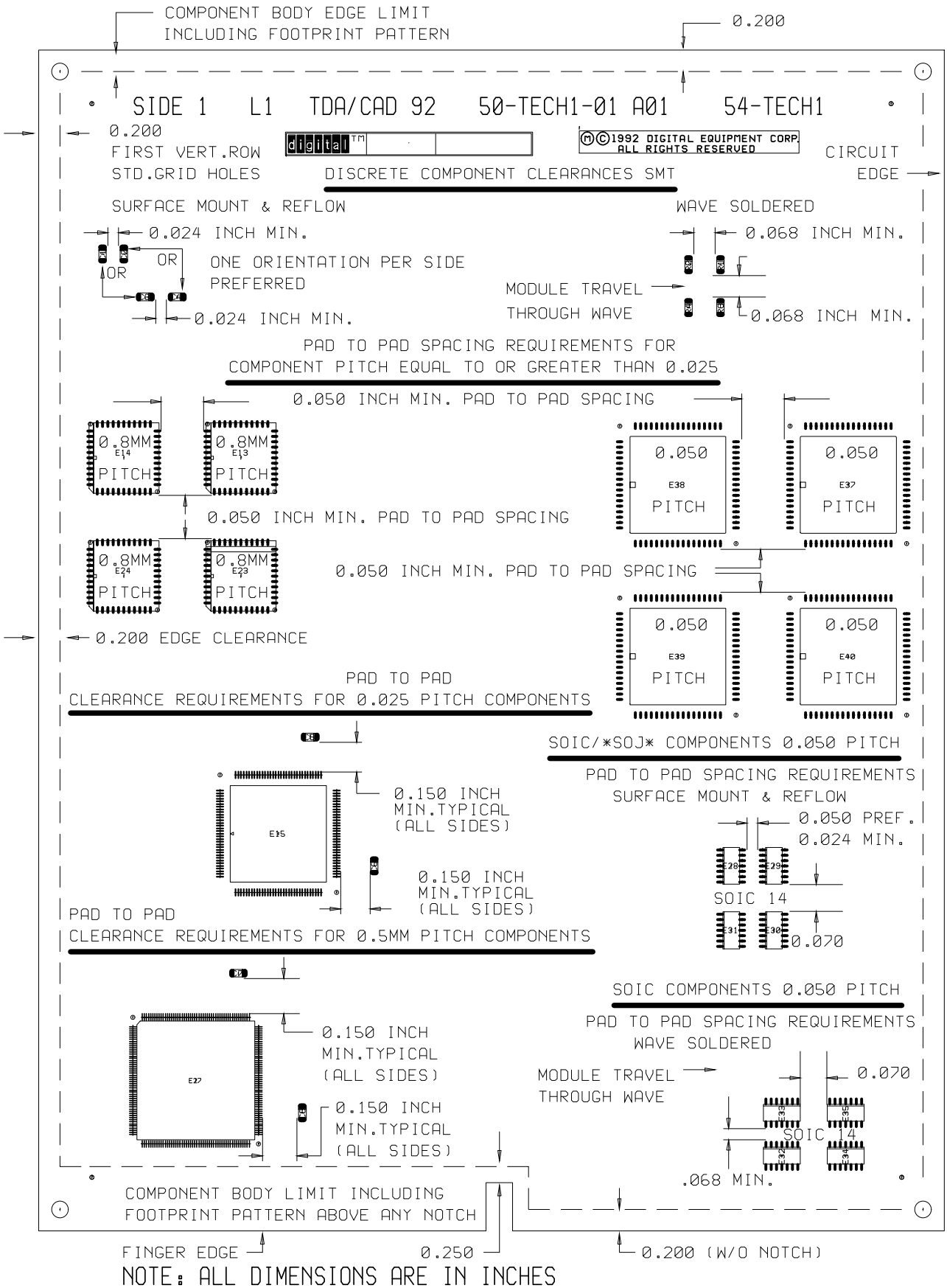


Figure 7-17: Through-Hole Component Clearances

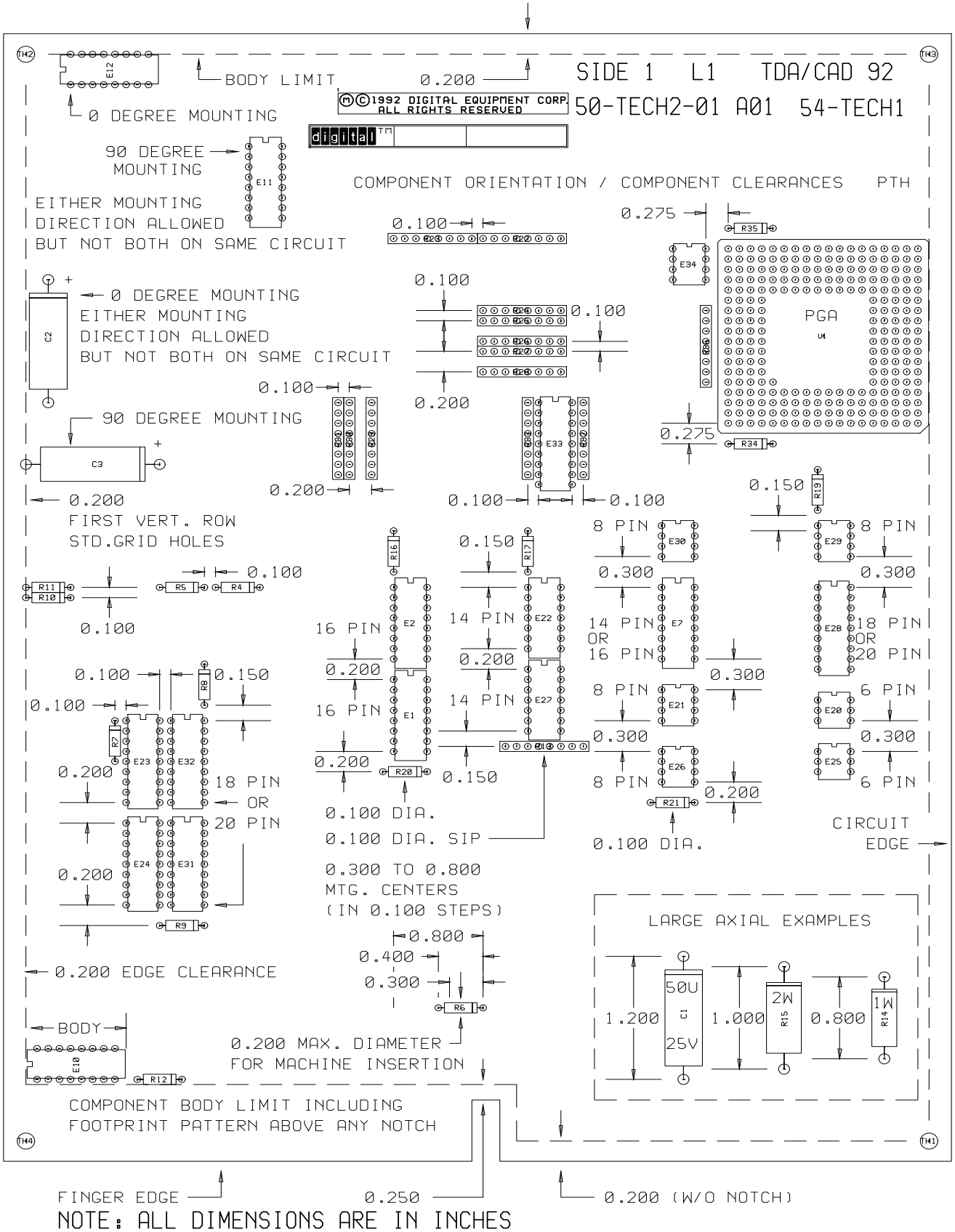


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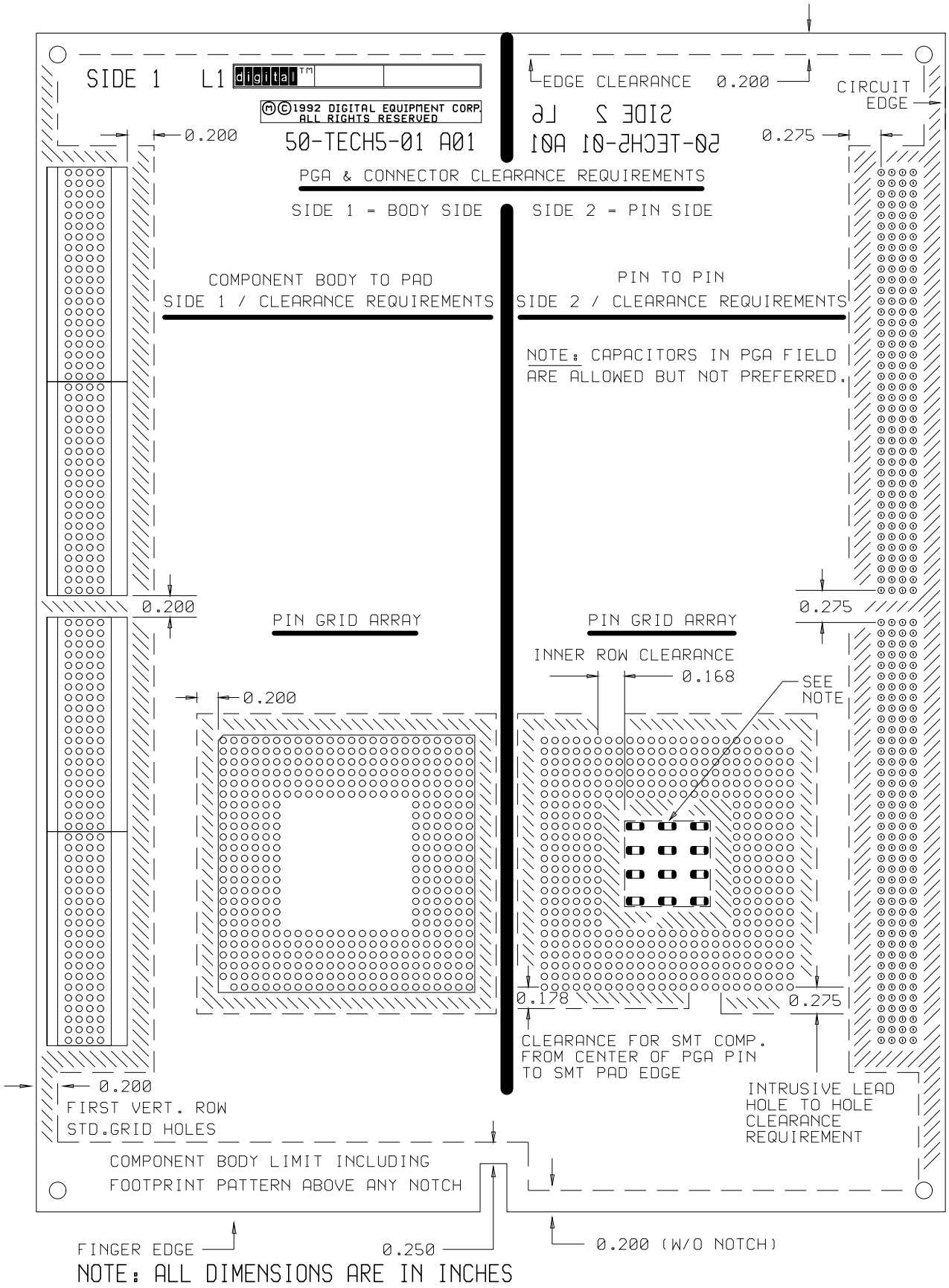
Figure 7-18: PGA and Connector Clearances



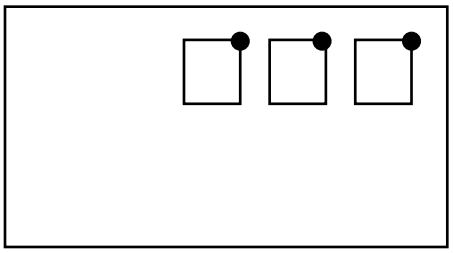
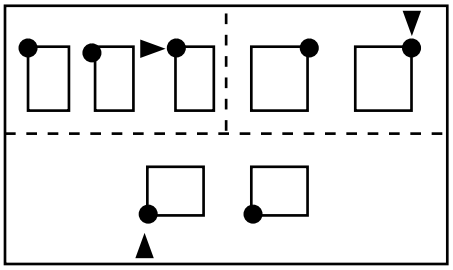
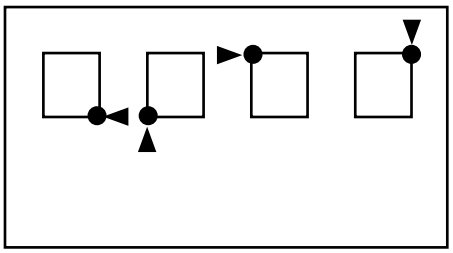
Rule 4-2 Component Orientation

It is preferred that all components are in the same orientation, with pin 1 in the same corner to facilitate the module inspection and ICT diagnose processes. See Figure 7-19 for alternative solutions.

Impact:

If components are not oriented in the same direction, inspection and ICT costs increase due to the extended time to confirm correct orientation and locate defective pins.

Figure 7-19: Component Orientation Alternatives

Preference	Component Orientation Alternatives	Impact
Preferred	 All Pin 1 Locations are in the same location.	No added cost
Acceptable	 Like components have the same pin 1 orientation, minimum of one component pad in each group marked with pin 1 orientation.	Increased inspection and ICT cost Additional defects may be found later in the process.
Acceptable	 Mixed Pin 1 Orientation, Pin 1 is marked on all components.	Increased Inspection and ICT cost Additional defects may be found later in the process.

Rule 4-3 Overhanging Component

Overhanging components are **not preferred**.

Known exceptions include: PTH and SMT connectors, LEDs, and switches that protrude through the system box. Use Figure 7-20 as a guide.

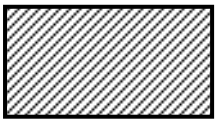
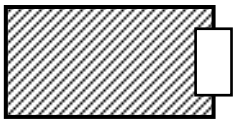
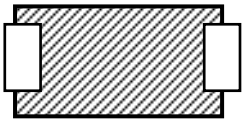
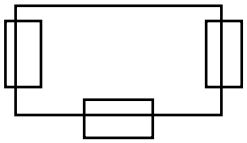
Impact:

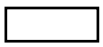
If overhanging components are present, one or more of the following costs may be incurred.

- Break-aways may be needed — $ 0.20 per break
- Final (post-wave) assembly — $1 to $10 per component
- Custom fixtures and handling — $30,000 to $70,000 per product plus $0.50 to $1.00 per module

If none of the above solutions are used, there will be an increase in defects during the solder wave process and potential damage to the overhanging components.

Figure 7-20: Overhanging Component Descriptions

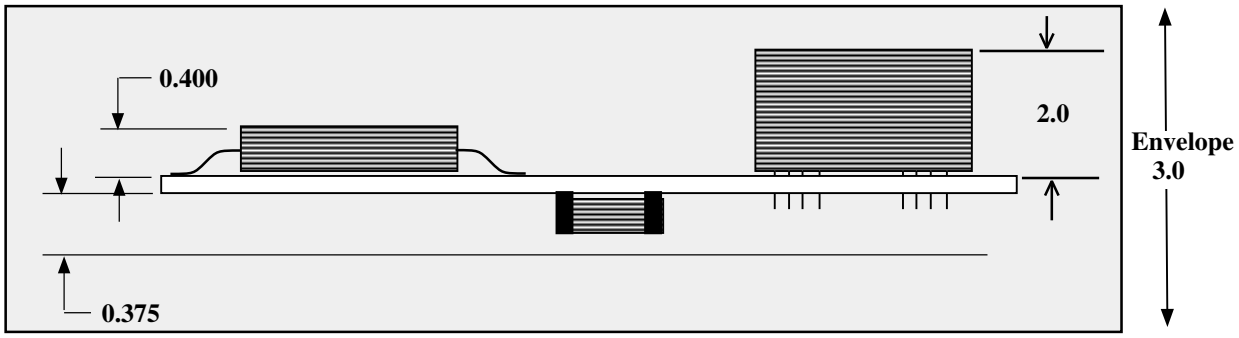
Preference	Design Description	Assembly Cost Impact
Preferred	No Overhang 	None
Acceptable	Overhang on either leading or trailing edge 	Low end of ranges listed above
Acceptable	Overhang on both leading and trailing edge 	Middle of ranges listed above
Acceptable	Overhang on multiple axes 	High end of ranges listed above

Module  Overhanging component

Rule 4-4 Module Height Equipment Constraints

Figure 7-21 shows module height restrictions based upon the entire manufacturing process. Note that because the through-hole assembly process is carried out after the surface mount assembly process, through-hole components can be higher than surface mount components on the same mixed-mount module.

Figure 7-21: PTH, SMT, Mixed Assembly Process Preferred Envelope



All dimensions are in inches

Process	Envelope	Side 1	Side 2
PTH	3.0	2.0	0.375[2]
SMT	2.0	0.400[1]	0.400[1] [2]
Mixed	3.0	per comp type	0.375[2]

[1] Some Manufacturng plants have placement equipment that will accommodate 0.600 inch. See **Section 7.6.2**.

[2] See **Rule 5-4** for ICT Side 2 Component Height Requirements.

Impact:

Final (hand) assembly is required at a cost of $1 to $10 per component if components cannot fit in process equipment.

The height constraints on a module are dependent on the module process flow. If the module stays within the recommended envelope, there will be no issue; however, if this cannot be accomplished, the Manufacturing Engineer can determine which process equipment height constraints apply to a given module based on the module assembly process flow. See **Section 7.6.2** for individual process element constraints.

Rule 4-5 Component Placement on Mixed Mount Module

The type, quantity and placement of PTH and SMT components on side 1 and side 2 of a mixed mount module affect the soldering process selection. In general, it is preferred to use the wave solder process over the selective solder process(Wenesco). Table 7-5 describes the soldering options available and the criteria for using that process.

Table 7-5: Soldering Process Criteria

Preference	Process	Criteria	Process Flow*
Preferred	Solder Wave	1. The design is single-sided mixed mount. 2. Only SMT discretes smaller than 1812 body size mounted on side 2.	A + C + B
Acceptable	Shielded Wave	PTH devices are located only on side 1 and positioned to allow use of a shield during the wave solder process. See Figure 22.	A+A+B+[C]
Acceptable	Selective Solder (low volume process)	See Section 7.6.3 Selective Soldering Guidelines.	A+A+D

* See **Section 7.6.1** for details of Assembly Process Flow description and cost summary.

The important aspect of the example below is that the SMT components mounted on side 2 are in an area which can be shielded from the solder. Note the ability to use straight or L-shaped shields.

Figure 7-22: Side 2 View of Component Grouping Example

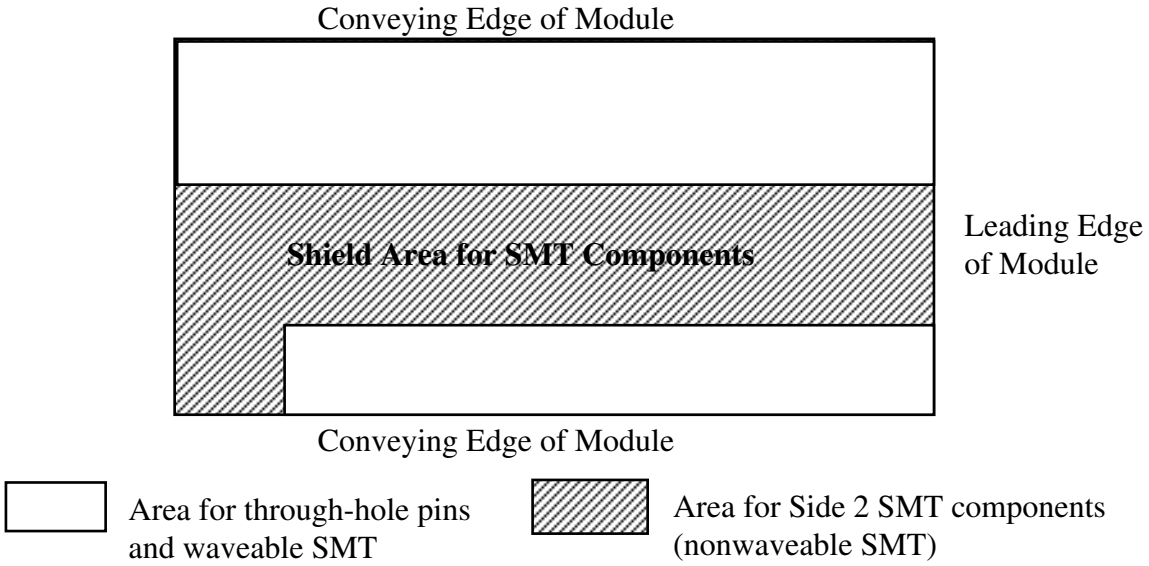

Conveying Edge of Module
Shield Area for SMT Components
Leading Edge of Module
Conveying Edge of Module
Area for through-hole pins and waveable SMT
Area for Side 2 SMT components (nonwaveable SMT)

Table 7-6 contains a list of component types and describes their compatibility with the soldering processes.

Table 7-6: Component Compatibility with Soldering Processes

Component Type	Solder Wave Compatable	Selective Solder Compatable
Side 2 SMT		
Chip Component		
≤ 1812 body size	Yes	No
≥ 1812 body size	No - Component Cracks	No
SOIC ≤ 16 pin[1]	Yes - but poorer yields	No
SOT 23	Yes - but poorer yields	No
Side 1 Through-hole		
All	Yes	Yes
Side 2 Through-hole		
All	No	Yes

All other SMT components on side 2 need to be SMT assembled and shielded if Solder Wave Process is used.

[1] Ensure components are compatible with wave solder process.

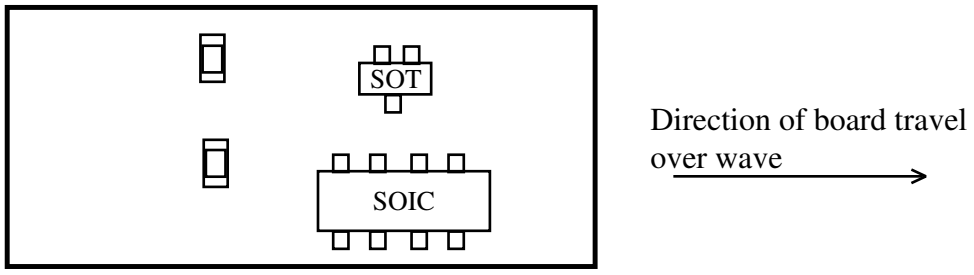
Impact:

The solder wave process is the preferred process because of cost and through-put; some manufacturing plants do not have a Selective Soldering Process in place. Module design complexity adds additional process steps and thermal cycles to the module assembly process. This impacts both process cost and quality and product reliability.

Rule 4-6 Side 2 Component Orientation for Wave Soldered Module

SMT Components on side 2 that are wave soldered should be oriented as shown in Figure 7-23. Wave Soldered SOICs have a special footprint pattern. See **Section 7.4.6**.

Figure 7-23: Side 2 Component Orientation



Note: SOT and SOIC packages are not preferred on Side 2 of a wave soldered module.

Impact:

Components oriented differently than as recommended can result in an increase in the number of defects per component of 1.5 to N, where N is the number of leads on the trailing edge.

7.2.5 In-Circuit Test

Adherence to the rules found in this section ensure the ability to perform in-circuit test.

Rule 5-1 Test Point Accessibility

Table 7-7 and 7-8 define test point accessibility for the following two requirements.

1. A minimum of one test point per signal network, including single point networks is required.
2. One test point for every 0.5 amps on power nets is required.

Table 7-7: Test Pad Size Pitch

Module Size (inch)	Nominal Test Pad Size (inch)	Test Point Pitch (inch)
≤ 12 x 16	0.035	0.050
> 12 x 16	0.040	0.070

Table 7-8: Clearance to Test Point Pad Edge to Component Body[1]

Component Height (inch)	Clearance to Test Point Requirement
≤ 0.200	0.020
> 0.200	0.080

Note: See Rule 3-2 for clearance to board edge requirements.

Impact:

Nonconformance results in :

- Decreased fault coverage and isolation at the ICT step or the exclusion of in-circuit test as a feasible test strategy.
- Increased rate of false failures and misdiagnosis at ICT results in increases in the number of retry opportunities to arrive at a correct diagnosis and the repair time per defect (more repair for the same number of true defects). This level of nonconformance increases the cost of the in-circuit test step by 10 to 15% per module.
- Elimination of the feasibility of ICT as a test process step passes all manufacturing-induced faults to functional test for detection. This increases the overall test cost per module by 4 to 7%.

[1] The clearance requirements for components greater than 0.200 inch assume that there are only a few of these large components on side 2 of the module.

Rule 5-2 Vacuum Fixturing Requirements

The standard strategy of ICT is to use a vacuum-actuated bed-of-nails fixture to contact test points on side 2 of the module.

The following two conditions **must** be satisfied for vacuum Automatic Test Equipment (ATE) fixturing to be used without a mechanical overclamp:

1. The maximum number of unfilled vias that may exist and still permit vacuum ATE fixturing to be used is:

   $$n = \frac{1.016 - 0.0136 * L}{\pi d^2}$$

   where

   n = number of unfilled vias
   d = diameter of via (inch)
   L = perimeter of circuit or vacuum seal (inch)

   Examples

Diameter of via	Maximum Number of Unfilled Vias
0.038 inch	234 - 3 * L
0.020	845 - 10.8 * L
0.010	3381 - 43.3 * L

2. Test probe density must not exceed an average of 20 probes per square inch of module area. This number accounts for counter acting vacuum force and includes allowances for vacuum leaks and fixture springs.

Impact:

If either of the two conditions above is not satisfied, a mechanical overclamp will be needed on the ATE fixture.

- The requirement for a mechanical overclamp adds to the price of the test fixture. The additional cost ranges from $375 to $2000 depending on the size of the module.
- The amount of on-machine diagnose time required at the ICT step increases due to the decreased accessibility to side one of the module. This decreased accessibility inhibits scratch probing, setting up scope loops, etc.
- The amount of time required for hardware tool development increases because stress simulations need to be performed to determine the placement of the hold-down pins within the overclamp. Overclamp design could also be required if the module profile prohibits the use of a standard overclamp.
- Nonconformance increases the in-circuit test cost per module by 10 to 14%

Rule 5-3 Mechanical Overclamp Clearance Requirements

The use of a mechanical overclamp requires 0.250 inch diameter areas on side 1 of the module to accommodate the following patterns free of components and side 1 etch.

Requirements:

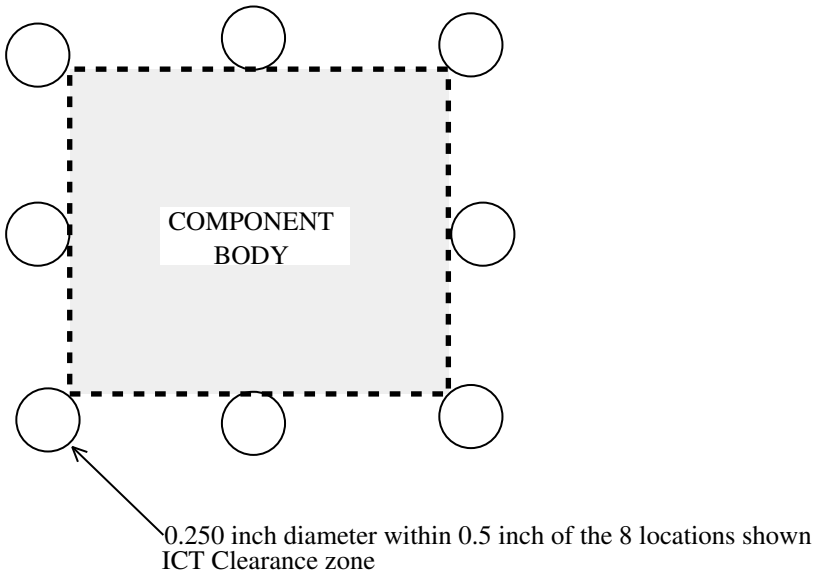
Packages with up to 200 pins:

One 0.250 inch diameter area per 3 square inch of board area
One 0.250 inch diameter area per every 25 test probes

High Pin count Packages:

- 200 to 400 pins:
  Probe only 50% of device pins
  Place eight hold-down pins around device or the perimeter of the heatsink, which ever is larger. The hold-down pins require on 0.250 inch area at each corner and at the center of each side of the device. See Figure 7-24.
- Greater than 400 pins:
  Probe only 200 device pins
  Follow guidelines in Figure 7-24 for hold-down pin placement
  Consult test engineer for stress analysis

Figure 7-24: High Pin Count Package Clearance Area for ICT



Connectors:

- 200 to 500 pins:
  One 0.250 inch diameter area per 25 test probes
  One 0.250 inch diameter area per 1.5 inches connector length
- 500 to 750 pins:
  One 0.250 inch diameter area per 25 test probes
  One 0.250 inch diameter area per 1.0 inch connector length
- PWB with gold fingers:
  One 0.250 inch diameter area per 30 test probes
  One 0.250 inch diameter area per 1.8 inch gold fingers
- PWB with corner cutouts close to connectors:
  See Test engineer for stress analysis.

Impact:

Nonconformance to the spacing or clearance requirements for ATE fixtures results in the following:

- Placement of hold-down pins used in ATE fixturing to offset the upward force of the test probes is restricted. This, in turn, results in restrictions on test probe placement. The acceptable level for probe density in a given area is decreased because the upward forces of the test probes without the compensating downward forces of the hold-down pins may damage the module.
- Some test points must be moved off of large pin count devices. In addition, areas of the module populated with a high density of components will need to have test points eliminated or moved to other accessible points on the network.
- Signal integrity problems may show as false failures. If test points are eliminated, it is necessary to test devices in clusters and fault isolation is degraded.
- The ICT cost per module increases by 25 to 28%.

Rule 5-4 Side 2 Component Height for ICT

Side 2 components must have heights of 0.225 inch or less to avoid routing of the fixture top plate.

Impact:

During in-circuit test, the module is placed on side 2 on a bed-of-nails test fixture. The G10 top plate in the fixture must be routed out to accommodate any side two components whose height is 0.225 inch or greater. This increases the expense of testing. Also, there is less mechanical guidance for the probes in the routed areas which can result in decreased contact reliability since the probes are more likely to deviate from a vertical stroke. If components with heights larger than 0.225 inch must be used, they should not be grouped together on the module. This will allow small pockets to be routed instead of one large area.

Nonconformance to this rule manifests itself in the following ways:

- Increased fixture cost due to the routing of the top plate.
- Decreased fixture contact reliability which causes an increase in the number of false failures experienced at the in-circuit test step.
- Increases in the number of retry opportunities to arrive at a correct diagnosis and the repair time per defect (more repair for the same number of true defects).

  As a result, test cost per module for the in-circuit test step increases by 10 to 15%.

Rule 5-5 Explicitly Created Test Pad Connections and Stub Lengths

Explicitly created test pads and stubs shall be connected as close to a driving node on the electrical network as possible.

Stub lengths for explicitly created test pads should be as short as possible to avoid signal delay. The following list details the **maximum** length for the silicon technologies in use today.

MCS, 100K, ECL, CMOS3, CMOS4	0.25 inch
10K ECL, FTTL, CMOSD2	0.50 inch
CMOS1, TTL, S TTL, HS TTL, LS TTL, MOS, CMOS, NMOS	1.0 inch

Stub length is measured from the center of the component or via pad to the center of the test pad.

Impact:

If stub lengths are longer than recommended, there is a risk to the functionality of the circuit due to signal delay.

7.2.6 Marking

The following rules define the requirements for marking on a module.

Rule 6-1 Required and Preferred Nomenclature

All nomenclature is preferred to be in etch. All required nomenclature must be in etch. See Table 7-9.

Table 7-9: Nomenclature Requirements

Feature	Example	Requirement
Required Markings		
Product safety frame and marking (outer layer only)	digital™	UL requirement Clear space for PWB vendor
Copyright and mask works protection (outer layer only)	© 1992 Digital Equipment Corp. **All Rights Reserved**	Copyright requirement Update with ECO
PWB part number and revison numbers (etch layer only)	50-12345-01 B01	Digital Corporate Requirement Refer to DEC STD 030-2
Module Number 54-12346-01 B01	54-12346-01 B01	Digital Corporate Requirement Refer to DEC STD 030-2
Layer identification Etch layers Ground and Power ID Power potential ID (on power layer)	L1, L2 GND,PWR +5V, -3V, -12V	PWB requirement
Preferred Markings		
Pin 1 Indicator (PTH)	Round pad replaced by square pad in etch on PTH	Assembly and repair
Pin indicator (SMT)	Isosceles triangle pointing to SMT pad in etch or screen	Assembly and repair
Polarity indicator	+ symbol at a capacitor anode - symbol at diode cathode	Assembly and repair
Reference designators	E, C, R, J, P, and so on.	Assembly and repair

Note: The only required feature for OEM products is the Product Safety Frame without the Digital logo.

The Underwriters Laboratories (UL) frame can be separated to fit on a dense module. Frame parts must be on the same side of a substrate. Please refer all exceptions to the legal department.

Impact:

- Cost of nonconformance is loss of certification and resulting inability to market the product.
- Possible loss of copyright protection.

Rule 6-2 Requirements for Etch Nomenclature

Use Table 7-10 for determination of appropriate line widths for etch nomenclature.

Table 7-10: Etch Nomenclature Line Widths

Base copper weight (oz.)	Minimum line width (inch)
≤ 0.50	0.004
> 0.50	0.010
> 1.0	0.012

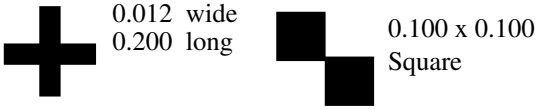
Impact:

Features that are too fine for a copper thickness result in poor legibility or possible removal of features during PWB manufacturing steps.

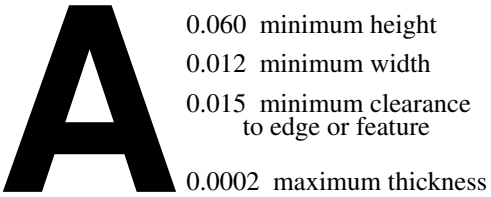
Rule 6-3 Requirements for Screened Nomenclature

- The minimum line width for nomenclature is 0.012 inch.
- Text height shall be 0.060 inch minimum.
- Minimum edge to edge clearance or to exposed conductive area is 0.015 inch.
- A minimum of two alignment targets placed on diagonally opposite corners must be included on the PWB to provide accurate registration of screened nomenclature.
- Screened nomenclature is not allowed on component pad.

Figure 7-25: Screened Nomenclature Illustrations



Nomenclature Size and Clearances



All dimensions are in inches.

Impact:

Deviation from these rules result in misregistration and smearing onto conductive areas.

Rule 6-4 Bar Code Area

An area on each module must be allocated for a bar code label for module traceability and in-process control. The preferred location for the barcode is on the side 1 conveying edge. Any edge on Side 1 is preferable to Side 2, but Side 2 edges are acceptable. See Table 7-11. If necessary, see DEC STD 047-0, Bar Code Symbology, for more information.

Table 7-11: Bar Code Area

Order of Preference	Number of Sites	Area Rquired (inches)	Bar Code Elements Priority
Peferred	Single site	0.250 x 5.26	Part number, Revison and Serial Number
Acceptable	Two Sites	0.250 x 5.5[1]	Revision and Serial Number
Acceptable	Three sites	0.250 x 5.76[1]	Serial Number only

Barcode Elements:

Single Site

1P 54-11111-01 *2P AB01* *1S CX24312345* Height 0.25 inch
IIIIIIIIIIIIIIIIIIII IIIIIIIIIIII IIIIIIIIIIIIIIIIIII Length 5.26 inch

Individual Elements

Part Number	*1P 54-11111-01* IIIIIIIIIIIIIIIIIIII	Height 0.25 inch Length 2.20 inch
Revision	*2P AB01* IIIIIIIIIIII	Height 0.25 inch Length 1.46 inch
Serial Number	*1S CX24312345* IIIIIIIIIIIIIIIIIII	Height 0.25 inch Length 2.10 inch

[1] Real estate increase is due to extra space required for additional quiet zones on each segment of the label.

Impact:

If bar code area is not allocated on a module, manual data entry is forced and there is an increased chance of human error and lot field traceability.

Note: Soldermask void area is 0.100 inch larger than the bar code area. See **Rule 7-6**.

7.2.7 Soldermask

The following rules concern the design and documentation of the soldermask layer of the PWB.

Rule 7-1 Soldermask Type

Liquid photoimageable soldermask (LPISM) is the preferred type of soldermask. See **Chapter 6, Printed-Wiring Boards.**

Impact:
Liquid photoimageable masks improves the quality during the module assembly process in these two ways.

- LPISM is thinner than other solder masks; this improves the screen printing process.
- LPISM 's resolution is such that when there is sufficient space, it allows soldermask to be placed between SMT component pads, which significantly reduces bridging during SMT reflow.

Rule 7-2 Soldermask Application

Soldermask must be applied to both sides of a module with finer than 0.012 inch lines and 0.013 inch spaces.

Soldermask must be applied to the solder side (typically side 2) of a module with line widths and spaces less than or equal to 0.020 inch.

Impact:

The use of soldermask eliminates conductor-to-conductor shorts that may occur during the module assembly process.

Rule 7-3 Soldermask Between SMT Pads

Soldermask should be designed between any SMT pads whose spacing is greater than or equal to 0.009 inch. This is the standard 0.025 inch package footprint with 0.016 inch pad and 0.009 inch space. Note that this can only be accomplished with the use of LPISM.

Impact:

Significant reduction in the quantity of assembly-induced shorts has been demonstrated through the use of mask between pads. This results in lower repair costs for the module.

Rule 7-4 Soldermask Void Areas

All conductive areas on the module should be covered with soldermask except the following void areas. Soldermask void areas should be designed at zero clearance.

- All vias and pads including test pads and component pads
- Fiducials
- Electrostatic Discharge (ESD) areas
- Gold Plating areas
- Conductor areas larger than 0.187 square inches on solder-plated boards (verses SMOBC or all copper)
- Bar code Void Area, 0.350 inch x 4.4 inches (or 0.100 inch greater than barcode length and width. See **Rule 6-4** Bar Code Area.)[1]

Note: The UL Block area **must** be covered by soldermask.

Impact:

It is necessary that these areas remain free of soldermask to enable the assembly, test and functionality of the module.

[1] If Bar code void area is not available, the bar code area must be a minimum of 0.500 inch away from any fine pitch component pads.

Rule 7-5 Soldermask Clearances

Use Table 7-12 to determine the clearance requirements for soldermask.

Table 7-12: Soldermask Clearance Requirements

Feature	Clearance Requirement (inch)
Circuit Edge	0.015
NPTH, cut-out or notch	0.015
Etch to SM Void Area	0.005
Void area to Void Area	0.013 (preferred) 0.009 acceptable

Impact:

A reduced clearance on routed or sheared edges creates the risk of soldermask flaking, which increases the cost of rework.

If void area clearances are not sufficient, there is an increased risk of soldermask lifting causing shorts and increases in repair cost.

Rule 7-6 Minimum Soldermask Width

The minimum soldermask width is 0.006 inch.

Impact:

Soldermask may lift causing increased opportunities for shorts during the assembly process and increased cost of repair.

7.2.8 Pad Expansion

Pad expansion is the addition of a smaller pad at the interface of an inner layer pad and etch to maximize the etch interface between pad and line if drill misregistration occurs.

Rule 8-1 Pad Expansion

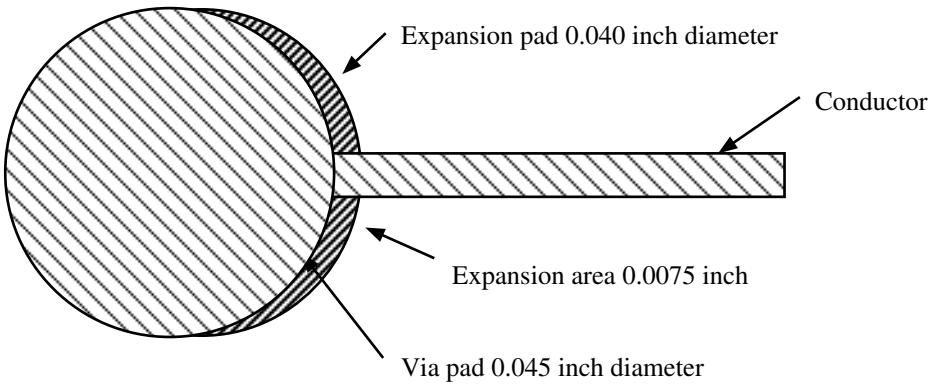
Pad expansion is **required** for any inner layer pad that connects to a line. Pad expansion is **not required** on outer layers

Use Table 7-13 to determine the size of the pad and extension that is required. See Figure 7-26.

Table 7-13: Pad Expansion Algorithm

Pad Size (inch)	Expansion Pad Size (inch)	Extension Beyond Pad (inch)
≥ 0.045	0.040	0.0075
≥ 0.040 - < 0.045	0.025	0.0065
≥ 0.020 - < 0.030	0.015	0.0065

Figure 7-26: Pad Expansion Illustration



Impact: Innerlayer drill breakout is reduced by the use of pad expansion.

Alternative:

If pad expansion cannot be easily done by the CAD system, all the pad sizes can be enlarged by 0.007 inch. This will also reduce drill breakout and take up more routing space.

7.2.9 Thieving

Thieving is a term that defines the addition of nonfunctional pads to equalize current distribution during the copper and tin-lead plating processes.

Rule 9-1 Thieving Pads for Outerlayers

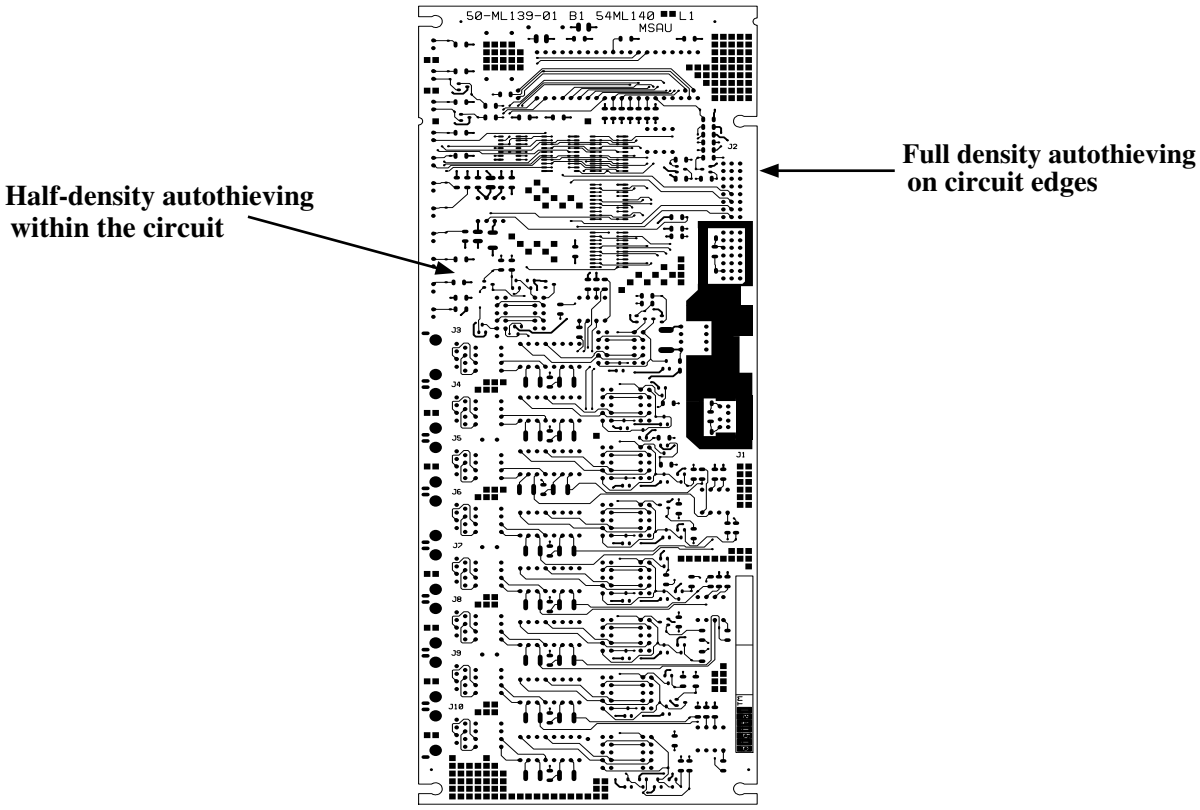
To ensure equalized distribution of nonfunctional conductor pattern, add thieving:

- In any open area
- To board areas that can be cut from the panel when the final outline is formed
- Around the perimeter of the isolated circuit and pad features

Thieving requirements:

- Thieving pads shall be no closer than 0.025 inch to circuit edge.
- Thieving pads are 0.080 inch square on 0.100 inch grid or 0.040 inch square on 0.050 inch grid.
- Thieving shall be full density with 1.00 inch inside the circuit outline, and half density over the remainder of the circuit. See Figure 7-27.
- Thieving pad shall be no closer than 0.05 inch to any other feature.
- For controlled impedance etch on adjacent layers, autothieving pads should be no closer than 0.050 inch to the conductor on the adjacent layer.

Figure 7-27: Thieving Configuration Illustration


50-ML139-01 B1 54ML140 L1
MSAU
Full density autothieving on circuit edges
Half-density autothieving within the circuit

Impact:

Improved plating distribution increases etch width and pad consistency so rejects due to overplating component holes are reduced.

7.2.10 Miscellaneous

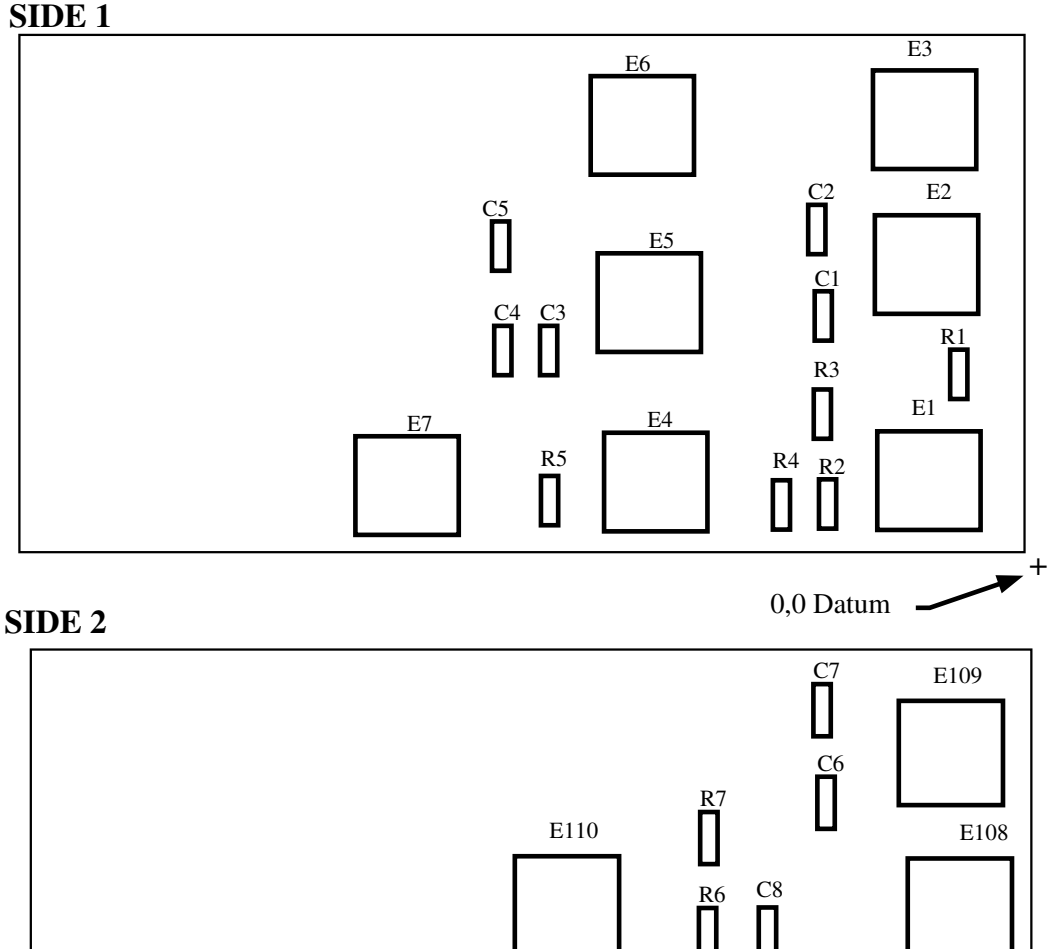
Rule 10-1 Integrated Circuit (IC)/Discrete Component Numbering Sequence

Both ICs and discrete components should be numbered from the 0, 0 Datum up the short end of the module, then to the left and up as shown in Figure 7-28.
Side 2 numbering should begin at the number following the last number on side 1.
(A gap of approximately 100 in the numbering sequence is recommended.)

It is preferred that components be numbered based upon its centroid position.

Note: Even if reference designators are not in the etch on the module, Unigraphics and CAD data should use this structure. Reference to logic schematic diagrams should be made for ease in test diagnostics. A listing of reference designators can be found in DEC STD 056-5 Industry Standard Logic Symbols and Diagrams.

Figure 7-28: Integrated Circuit/Discrete Component Numbering



Impact:

Inspection and test diagnostic time is increased if no order or sequence is used. If not in some order, all designators must be in etch.

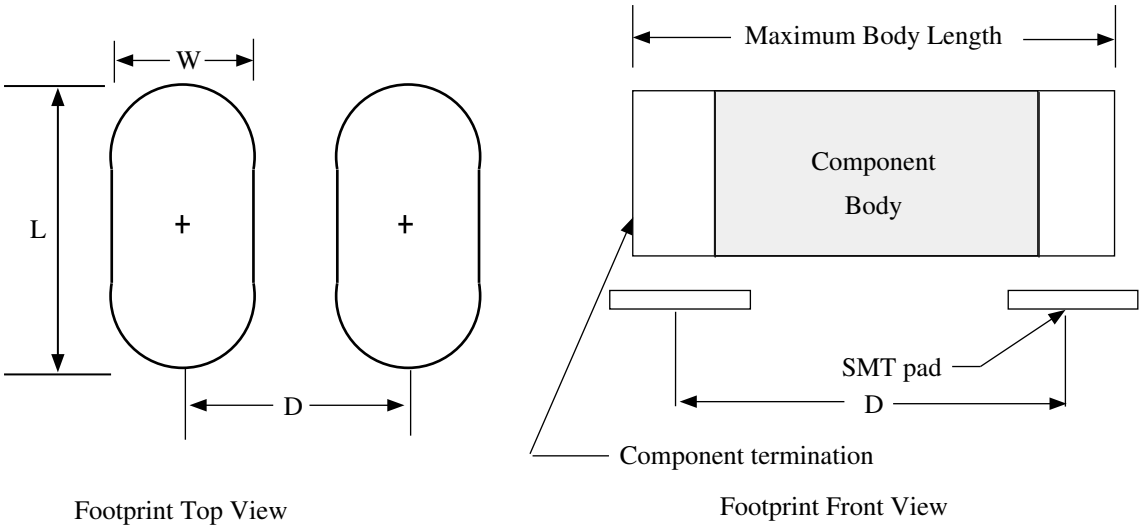
7.3 SMT Footprints

Each of the following pages describes the footprint patterns required for each SMT component style. All measurements are in inches unless specified otherwise.

7.3.1 Chip Component Footprint

For chip component foot prints that comply with A-PS-1000105-GS and A-PS-1300013-GS, refer to Figure 7-29 and Table 7-14.

Figure 7-29: Chip Component Footprint



Use the footprint calculations or Table 7-14 for these standard SMT chip styles.

Table 7-14: Chip component Pad Diemensions

Chip Style	W (inch)	L (inch)	D (inch)
0805	0.050	0.070	0.080
1206	0.050	0.082	0.126
1210	0.060	0.124	0.120
1812	0.060	0.150	0.170
1825	0.060	0.276	0.180

Footprint and Pad Calculations:
Pad Length (L) = Maximum terminal dimension +0.010 inch
Pad Width (W) = Maximum terminal dimension +0.020 inch
Dimension (D) = Maximum body length dimension +0.040 inch - (W)

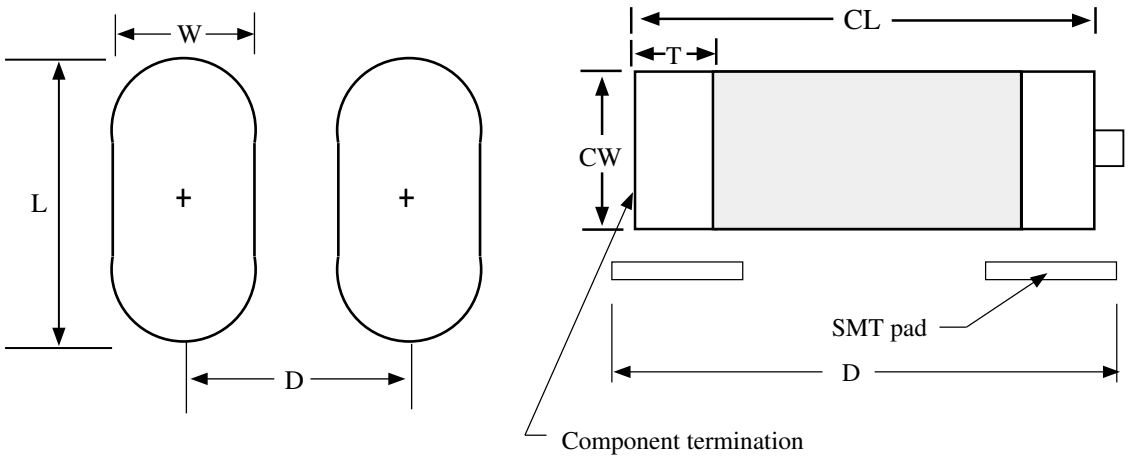
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.2 High Frequency Tantalum Capacitor Footprint

For high frequency tantalum capacitor footprint patterns that comply with A-PS-1000106-GS, use Figure 7-30 and Table 7-15.

Figure 7-30: High Frequency Tantalum Capacitor Footprint Design



Footprint Top View Footprint Front View

Use the footprint pad and spacing dimensions for these standard component styles.

Table 7-15: High Frequency Tantalum Capacitor Footprint and Pad Dimensions

Component Style	CW	CL[1]	T	W (inch)	L (inch)	D (inch)
A	0.065	0.110	0.040	0.060	0.076	0.090
B	0.065	0.165	0.040	0.060	0.076	0.146
D	0.100	0.145	0.055	0.076	0.110	0.110
E	0.100	0.215	0.055	0.076	0.110	0.180
F	0.145	0.230	0.055	0.076	0.156	0.194
G	0.115	0.275	0.075	0.096	0.126	0.220
H	0.165	0.275	0.075	0.096	0.176	0.220
Z	0.115	0.270	0.060	0.080	0.126	0.230

[1]Body size is measured without nub.

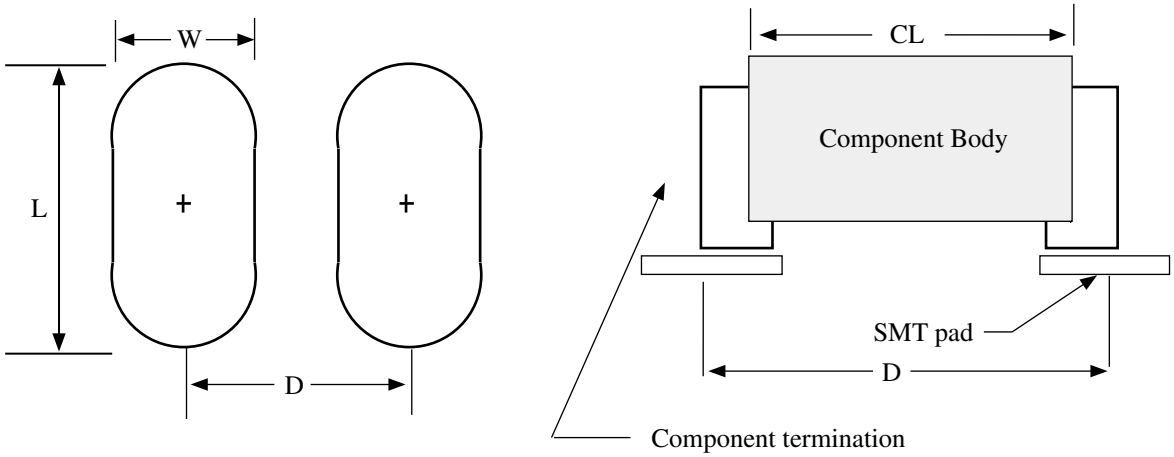
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.3 General Purpose Tantalum Cap

For general purpose tantalum caps that comply with A-PS-1000106-GS, use Figure 7-31.

Figure 7-31: General Purpose Tantalum Cap Footprint Design



Footprint Top View

Footprint Front View

Table 7-16: General Purpose Tantalum Cap Footprint and Pad Dimensions

Component Style	CL	TW	TL	W	L	D
A	0.134	0.051	0.043	0.064	0.062	0.110
B	0.146	0.091	0.043	0.064	0.102	0.122
C	0.248	0.091	0.063	0.084	0.102	0.204
D	0.299	0.099	0.063	0.084	0.100	0.256

TW = Termination Width
TL = Termination Length

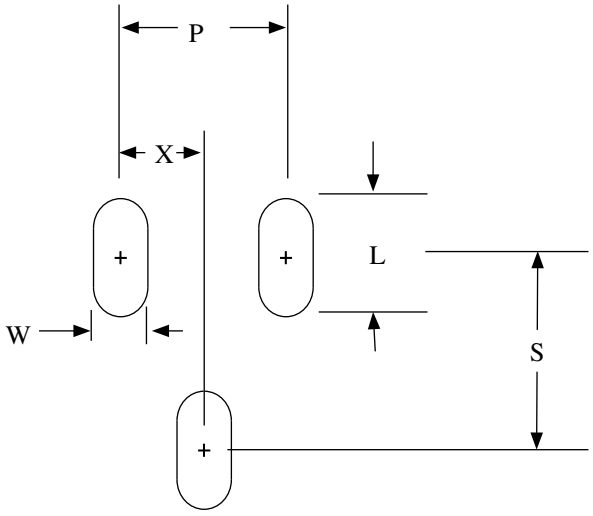
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.4 Small Outline Transistor (SOT) Footprint

For Small Outline Transistor (SOT) footprint patterns that comply with A-PS-1100006-GS, A-PS-1100007-GS, and A-PS-1100008-GS, use Figure 7-32.

Figure 7-32: SOT Footprint Design



Top View

Footprint and Pad Calculations:	SOT-23
Pad pitch (P) = Component lead pitch	0.076
Pad Spacing (S) = Lead span (maximum tip-to-tip)	0.110
Pad pitch (X) = 0.5*P	0.038
Width (W) = 0.040	0.040
Length (L) = 0.056	0.056

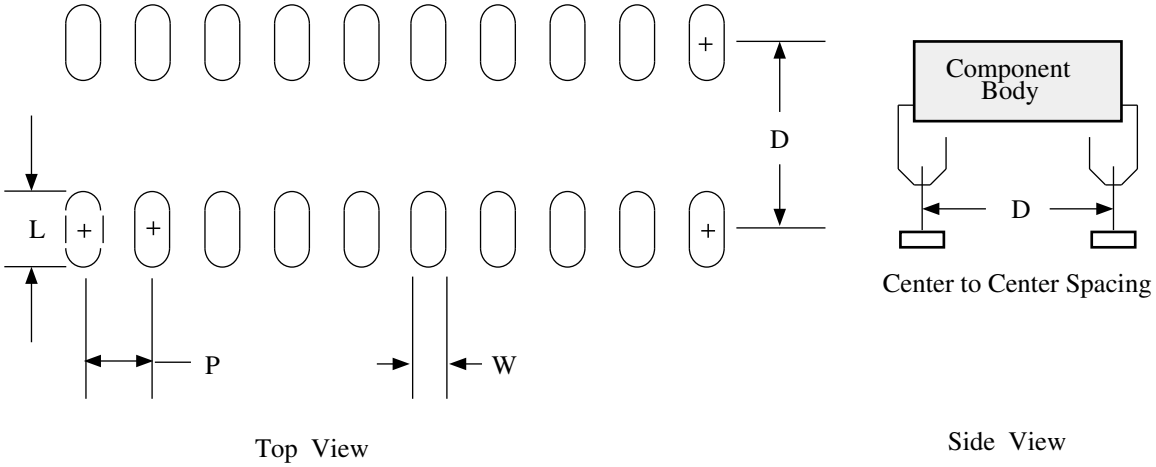
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.5 Small Outline J-Bend Component Footprint (SOJ)

For small outline J-bend component footprint patterns that comply with A-PS-1900032-GS, use Figure 7-33.

Figure 7-33: SOJ Component Footprint Design



Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch = 0.050 inch
Pad Center to Center distance (D) = Maximum component lead contact
Pad Width (W) = 0.030
Pad Length (L) = 0.076

Note:

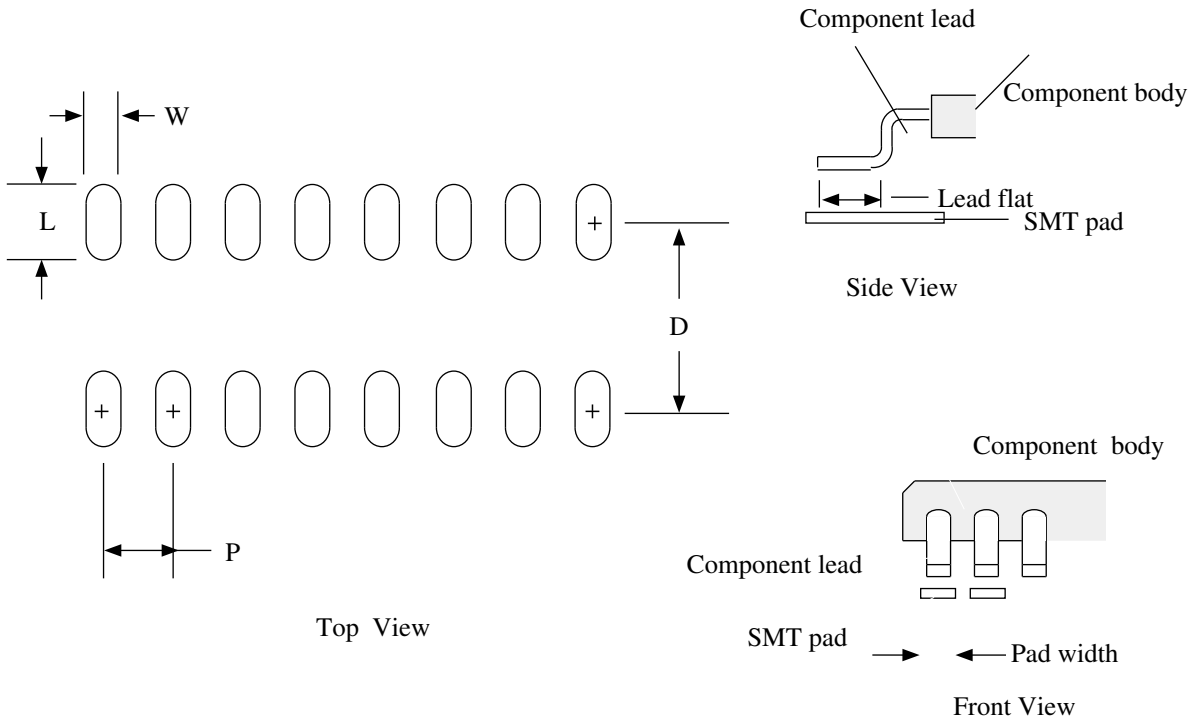
If pins are missing, such as on SRAMs and DRAMs, then drop the missing pin's footprint pad.

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.6 Small Outline IC Component Footprint (SOIC) for SMT Reflow

For small outline IC component footprint patterns that comply with A-PS-1900017-GS, use Figure 7-34.

Figure 7-34: SOIC Footprint Design for SMT reflow



Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch = 0.050 inch
Pad Width (W) = 0.030
Pad Length (L) = 0.076
D = Maximum Tip-to-Tip + 0.040 inch - (L)

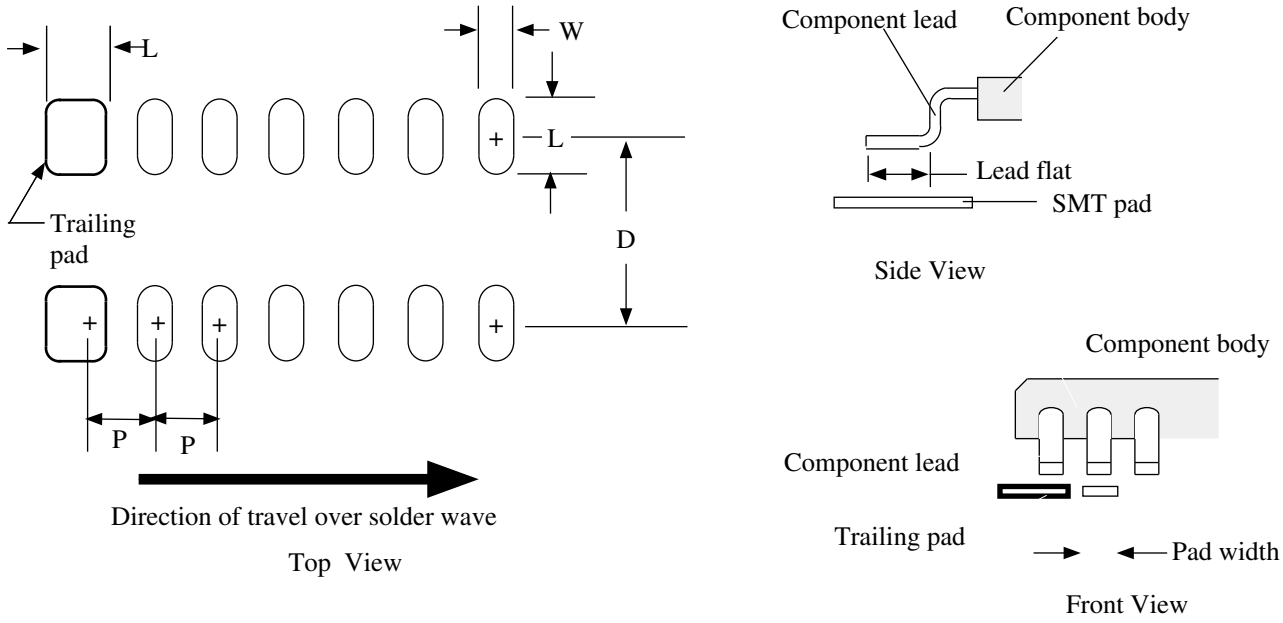
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.7 SOIC - Wave Solder Side 2 Footprint

For an SOIC that is to be wave soldered (typically on side 2) in compliance with A-PS-1900017-GS, refer to Figure 7-35. To reduce the chance of solder bridging over the solder wave, the trailing pad width is equal to the pad length (L). This is **not** a dummy pad.

Figure 7-35: SOIC - Wave Solder Side 2 Footprint Design



Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch = 0.050 inch
Pad Width (W) = 0.030
Pad Length (L) = 0.076
D = Maximum Tip-to-Tip + 0.040 inch - (L)

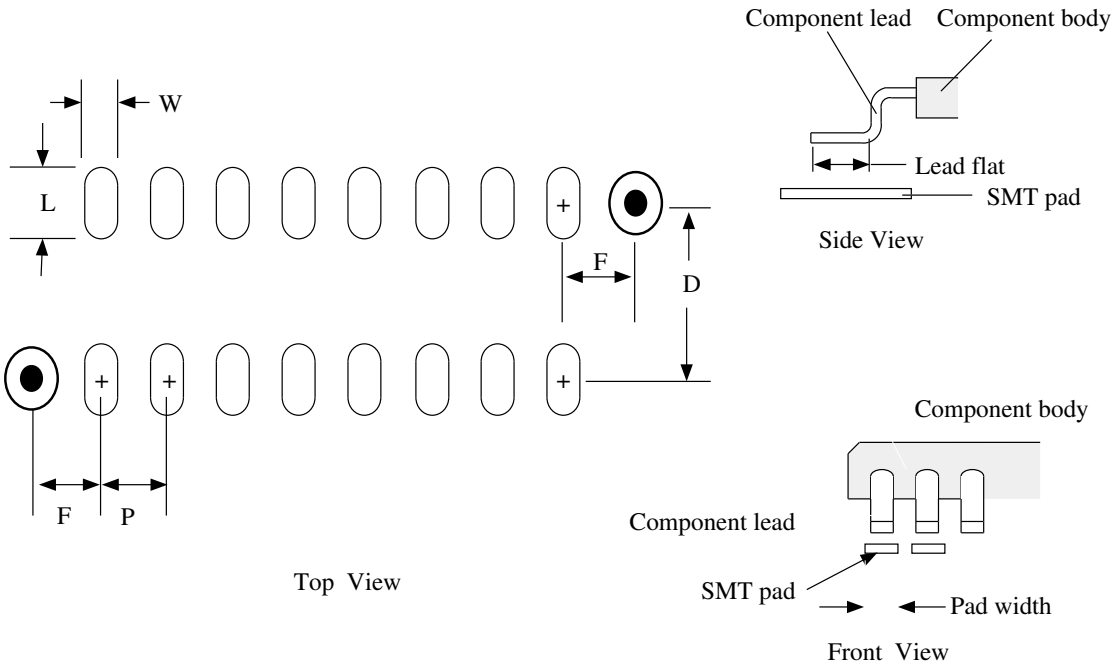
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.8 Shrink Small Outline Package (SSOP) Footprint

For shrink small outline package (SSOP) footprint patterns that comply with A-PS-190045-GS, use Figure 7-36.

Figure 7-36: SSOP Footprint Design



Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch = 0.025
Pad Length (L) = 0.076
Pad Width (D) = 0.016
Pad Dimension (D) = Maximum Component lead span + 0.040 inch - (L)
Fiducial location (F) minimum = 0.070 inch

Note:

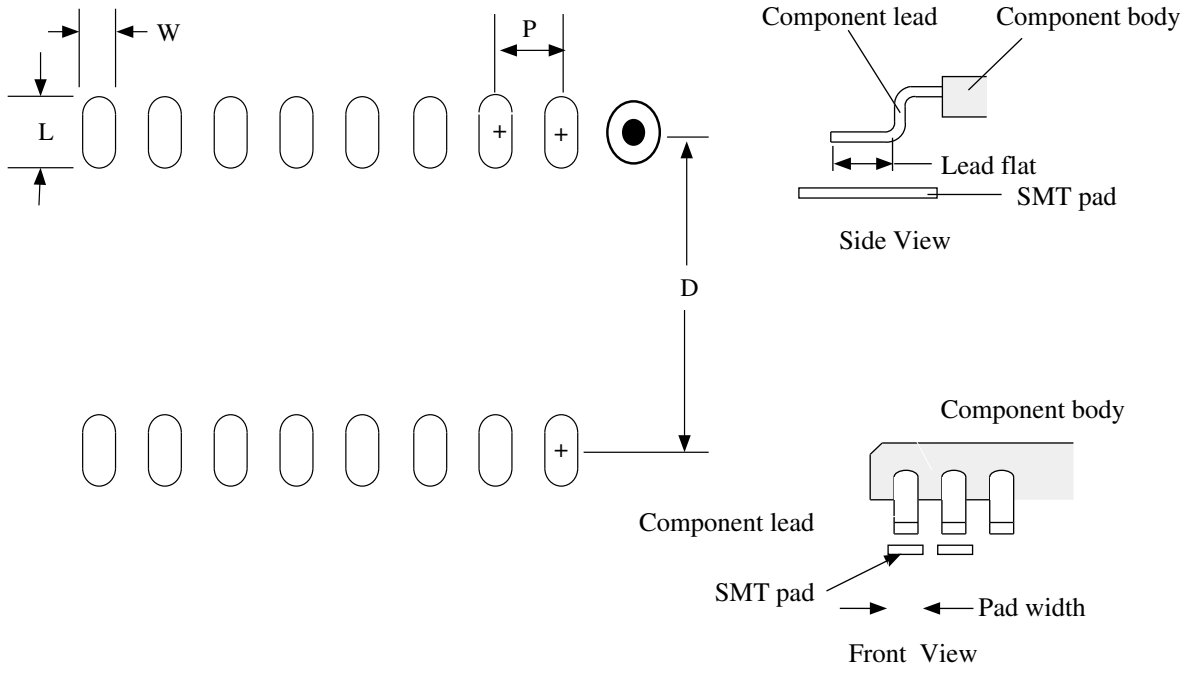
See **Rule 2-5** for Alternatives for fiducial location that may be necessary for this component type.

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.9 Thin Small Outline Package (TSOP-I)

For the small outline package footprint patterns that comply with A-PS-1900046-GS, use Figure 7-37.

Figure 7-37: Thin Small TSOP Outline Package



	Type-I	
	32-Pin	40-Pin
Pad Pitch (P) =	Component lead pitch	
Pad Width (W) =	0.012	0.012
Pad Length (L) =	0.050	0.050
Pad Centers (D) =	0.790	0.790

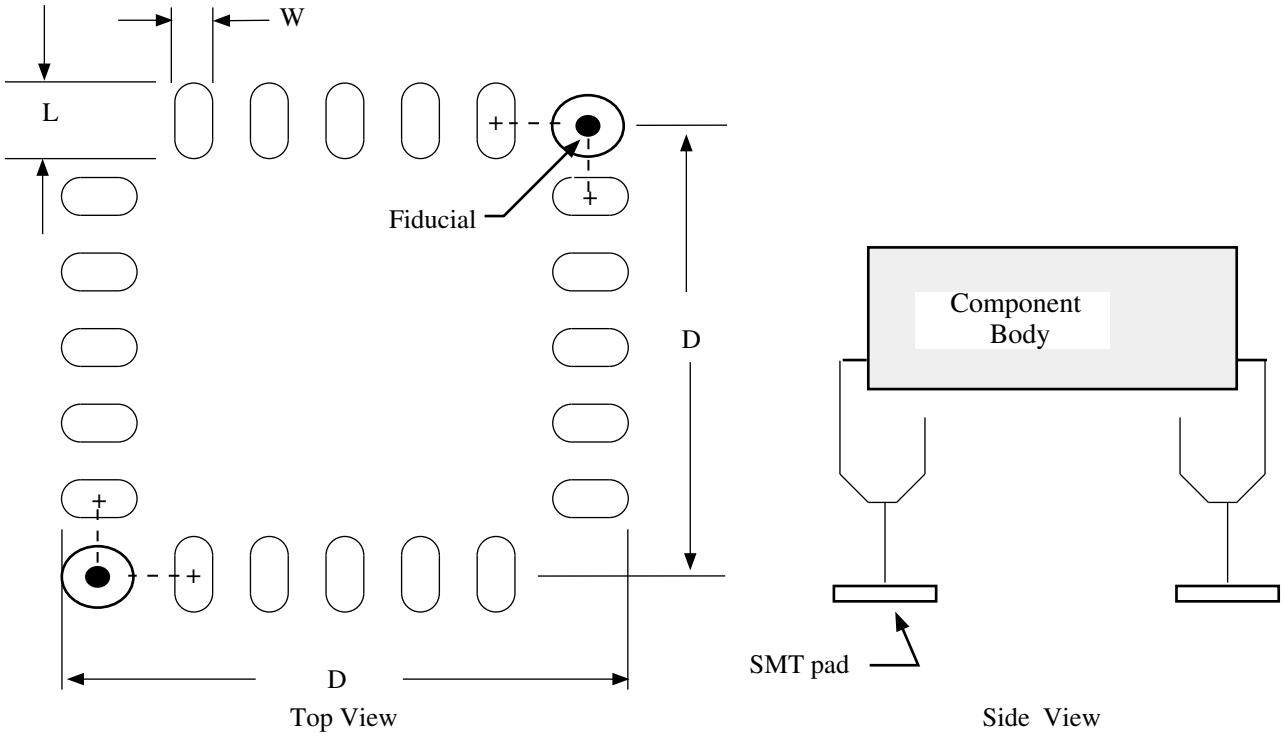
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.10 Plastic Leaded Chip Carrier 0.050 inch pitch (PLCC) Footprint

For plastic leader chip carrier (PLCC) footprint patterns that comply with A-PS-1900013-GS, use Figure 7-38.

Figure 7-38: PLCC Footprint Design



Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch = 0.050
Pad Center-to-Center distance(D) = Maximum component lead contact
Pad Width (W) = 0.030
Pad Length (L) = 0.076

* Fiducial not needed for 28 pin PLCC

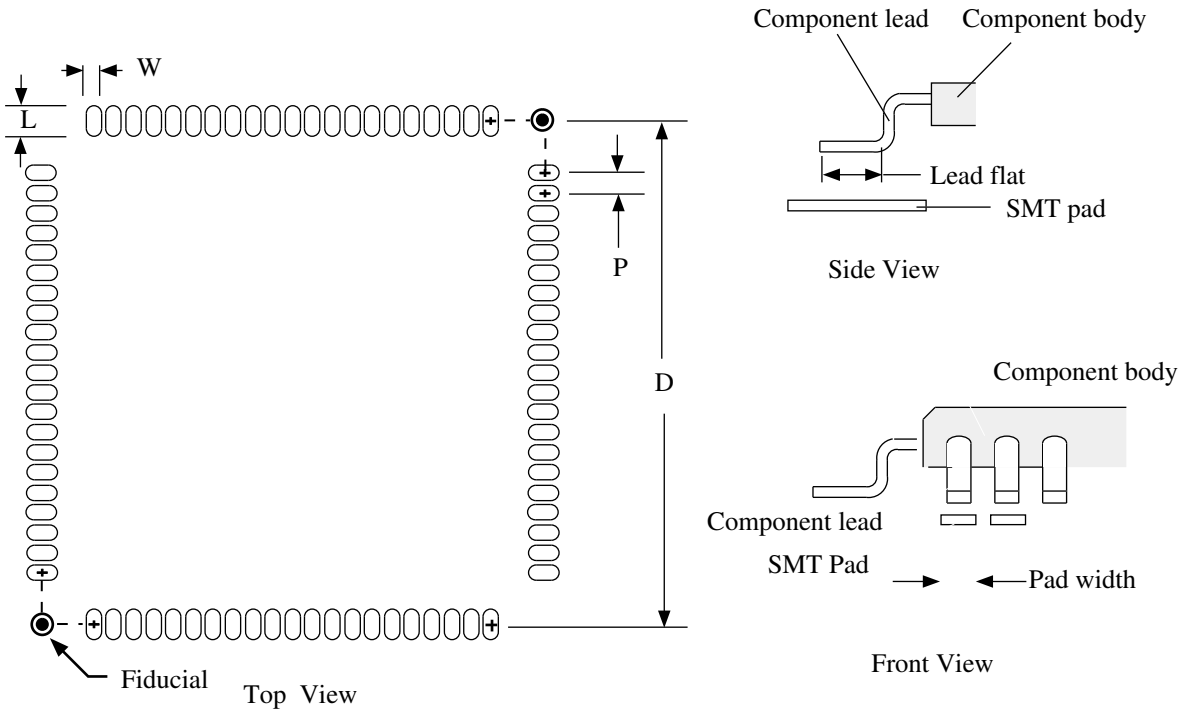
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.11 Ceramic Quad Gull-wing Package Footprint

For ceramic quad gull-wing package footprint patterns that comply with A-PS-1900031-GS and A-PS-1900034-GS, use Figure 7-39.

Figure 7-39: Ceramic Quad Package Footprint Design



Use the footprint and pad calculations or Table 7-22 for these standard package styles.

Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch
D = Maximum Lead Tip-to-Tip + 0.040 inch - (L)

Pitch (inch)	W (inch)	L (inch)
0.050 0.025	0.030 0.016	0.076 0.076

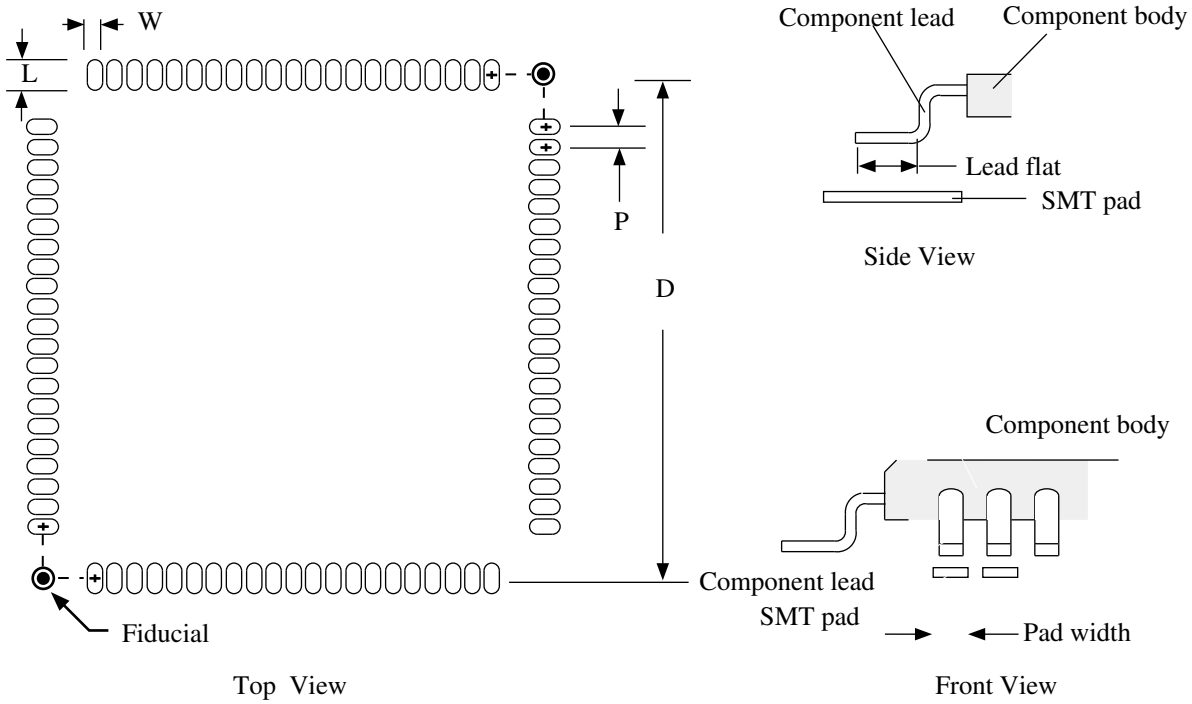
Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

7.3.12 Plastic Quad Flat Pack Footprint

For plastic quad flat pack footprint patterns that comply with A-PS-1900023-GS and A-PS-1900048-GS, use Figure 7-40 and Table 7-17.

Figure 7-40: Plastic Quad Flat Pack Footprint Design



Use the footprint and pad calculations and Table 7-23 for PQFP package styles.

Table 7-17: Plastic Quad Flat Pack Footprint Pad Dimensions

P (mm)	W (inch)	L (inch)
0.080	0.018	0.085
0.065	0.016	0.085
0.050	0.013	0.090

Ensure that metric components utilize a 0.0001 inch grid.

Footprint and Pad Calculations:
Pad pitch (P) = Component lead pitch.
(D) = Maximum lead tip-to-tip + 0.040 inch (1.0 mm) - (L)

Note:

For specific dimensions for all SMT components, refer to KELVIN::DISK$USER3:[TECHFILES.FOOTPRINTS].

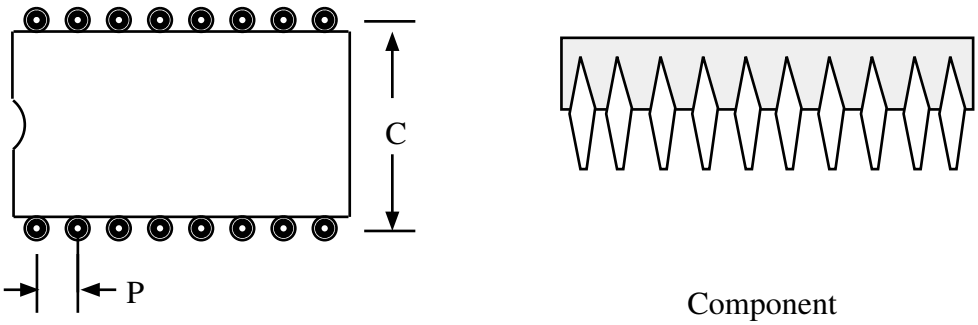
7.4 Through-hole Footprints

Use the following footprint patterns for these standard through-hole components. For components not found in this section refer to Section 7.5.9 for calculation PTH size.

7.4.1 Dual In-line Package (DIP)

For dual In-Line Package (DIP) footprint patterns that comply with A-PS-1900000-GS, use Figure 7-41 and Table 7-18.

Figure 7-41: DIP Component Footprint



Component Outline and Footprint Pattern Bottom View

Component Side View

Table 7-18: DIP Component Footprint Dimensions

Package Style	P (inch)	Finished Hole Size (inch)	C (inch)	Signal Pad Size	Clearance Pad Size
0.3	0.100	0.038	0.300	0.058	0.073
0.4	0.100	0.038	0.400	0.058	0.073
0.6	0.100	0.038	0.600	0.058	0.073

7.4.2 Axial

For axial-leaded device footprint pattern designs that comply with A-PS-1000001-GS and A-PS-1000106-Gs, use Figure 7-42 and Table 7-19 and Lead Mounting Center Calculation.

Figure 7-42: Axial Component Footprint

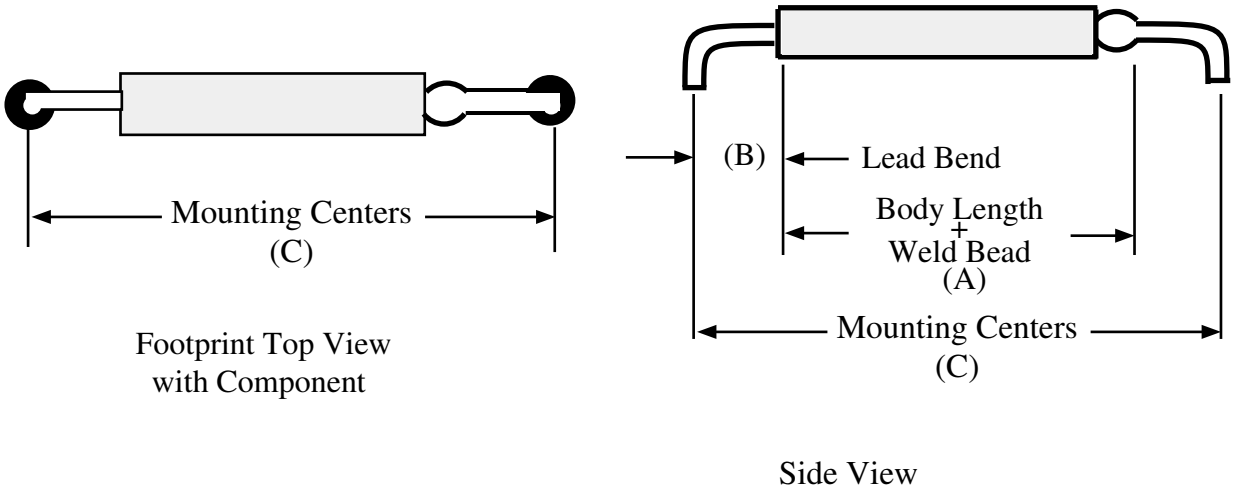


Table 7-19: Common Axial Component Lead Mounting Centers and FHS[1]

Component Body Diameter (inch)	Insertion Process	Lead Mounting Center(C) (inch)	Finished Hole Size (inch)
Less than or equal to 0.200	Automatic	0.300, 0.400, 0.800	0.038
0.200 or greater	Manual	0.800, 1.000, 1.200	0.038

Lead Mounting Center Calculation:

Lead Mounting Center (C) = Body + Weld Bead Length (A) + 2*Lead Bend(B)

B = 0.075 inch for body size ≤ 0.020 inch

or

B = 0.125 inch for body sizes > 0.200 inch

[1] See **Rule 2-1** Table 2 for Outer Layer Pad Diameter dimension based on Finished Hole Size (FHS).

7.4.3 Single In-line Package (SIP)

Use Figure 7-43 and Table 7-20 for SIP component footprint design.

Figure 7-43: SIP Component Footprint

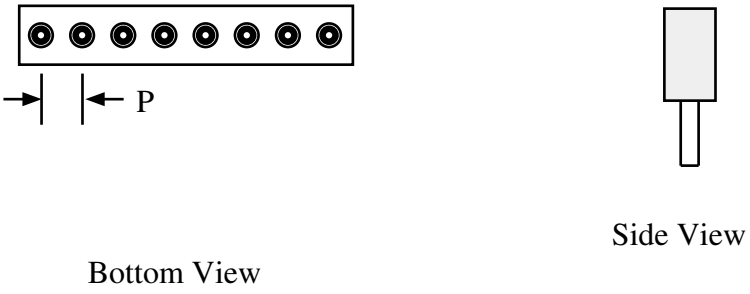


Table 7-20: SIP Footprint Dimensions

Package Style	P (inch)	Finished Hole Size (inch)	Signal Pad Size	Clearance Pad Size
SIP	0.100	0.038	0.058	0.073

7.4.4 Zig-Zag In-line Package (ZIP)

Use Figure 7-44 and Table 7-21 for ZIP components.

Figure 7-44: ZIP Component Footprint

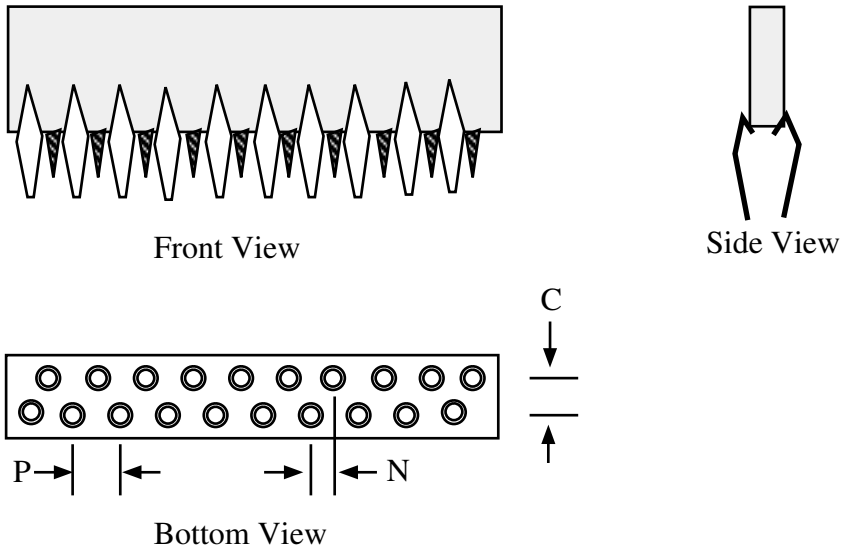


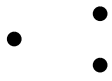
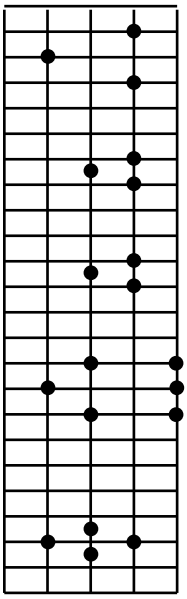
Table 7-21: ZIP Component Footprint Dimensions

Package Style	P (inch)	N (inch)	C (inch)	Finished Hole Size (inch)	Signal Pad Size	Clearance Pad Size
ZIP	0.100	0.050	0.100	0.038	0.058	0.073

7.4.5 Transistor

Use Figure 7- 45 for transistor package PTH locations.

Figure 7-45: PTH Transistor Layout Pattern

TRANSISTOR	PACKAGE LEAD PATTERN	LEAD PATTERNS ON GRID	PIN SIZE	HOLE SIZE
THREE LEADS: TO-5		0.200-0.200	0.026	0.038
TO-39				
TO-18		0.100-0.100	0.026	0.038
TO-92		0.100-0.100	0.026	0.038
TO-226				
TO-220		EITHER[1] 	0.032	0.042
TO-126				
FOUR LEADS: TO-72		0.100-0.200		

[1] Use left hand lead pattern for free standing TO-220

Use of the specified grid assures that the transistor stands off the PWB for etch clearance, this eliminates the need for transipads and saves $.10 - $.20 per part.

7.4.6 Pin Grid Array (PGA)

To design PGA component footprints that comply with A-PS-1900019-GS, and A-PS-1900010-GS, and A-PS-1900015-GS, use Figure 7-46 and Table 7-22.

Figure 7-46: PGA Footprint Design

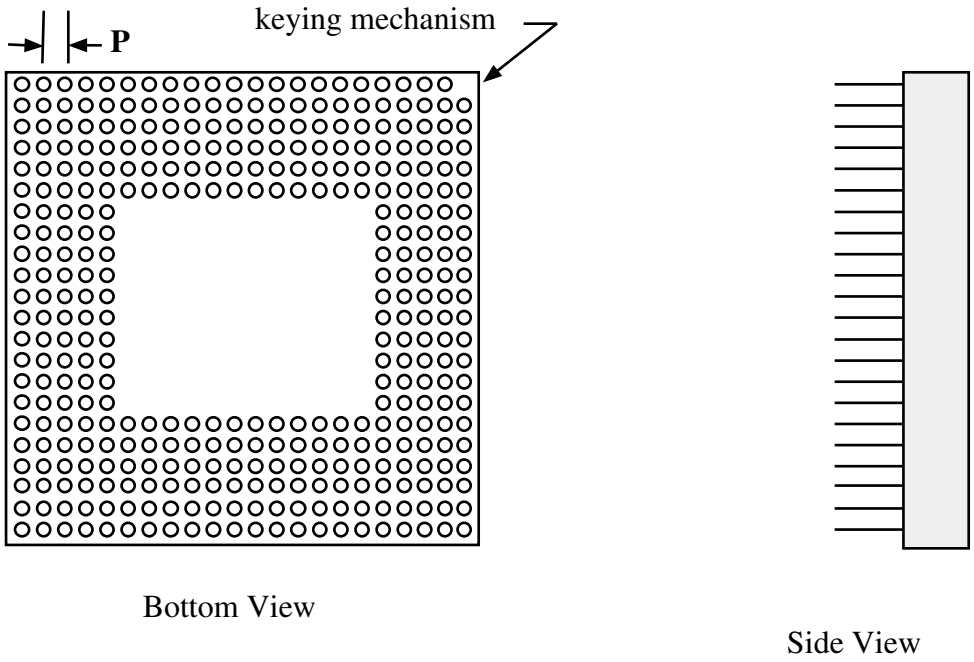


Table 7-22: PGA Footprint Dimensions

Pin Count	Pitch (P) (inch)	Finished Hole Size (inch)	Signal Pad Size	Clearance Pad Size
84	0.100	0.038	0.058	0.073
124	"	"	"	"
184	"	"	"	"
224	"	"	"	"
256	"	"	"	"
339	"	"	"	"
431	"	"	"	"

7.4.7 Interstitial Pin Grid Array (IPGA)

Use Figure 7-47 and Table 7-23 to design IPGA component footprints.

Figure 7-47: IPGA Footprint Design

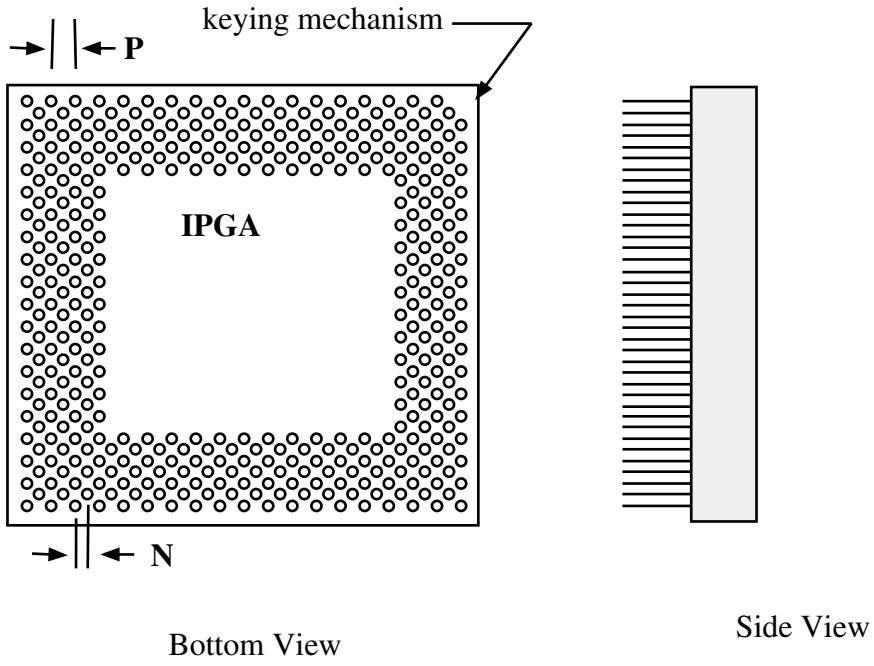


Table 7-23: IPGA Footprint Dimensions

Pin Count	P (inch)	N (inch)	Finished Hole Size (inch)	Signal Pad Size (inch)	Clearance Pad Size (inch)
391	0.100	0.050	0.028	0.043	0.053
447	0.100	0.050	0.028	0.043	0.053
503	0.100	0.050	0.028	0.043	0.053

Note: Pad Sizes are an exception to **Rule 2-1**.

7.4.8 Miscellaneous Nonmachine Insertable Through-Hole Components

Use Table 7-24 to determine hole sizes for the following components:

Table 7-24: Hole Sizes

Component	Hole Size (inch)	Pin Size (inch)
DIP Switch	0.038	0.025
40 Pin Header square pin	0.042	0.025 square
40 Pin Header round pin	0.038	0.025 round
IC Standard Socket	0.038	0.020-0.025
Crystal Oscillator Metal Can	0.032	0.018
Stake Pins	0.040 +0.003/-0.002 inch in 0.0093 inch thick PWB 0.032 ±0.002 inch in 0.062 inch thick PWB	0.025 square
Press Pin Connector	0.041 +0.002/-0.003	0.025
F-Bus Metral Press Pin[1]	0.026 -0.031	0.022
F-Bus Soldered Connector[2]	0.030 ±0.003	

Impact:

If hole is greater than 0.020 inch larger than the lead, then the joint will not solder correctly. If the hole is less than 0.007 inch then the lead, then the leads, holes, or both, will be damaged during insertion.

Caution: Review component specifications to verify dimensions.

Note: For other PTH components not covered in this section see **Section 7.5.9**.

1. Drilled hole size 0.033 - 0.034, copper plating 0.001 inch min, tin-lead (fused) 0.00015 minimum at crest.
2. Refer to K-MD-ELEN654-0-DBU, B Series Module Conector Detail and Circuit Outline.

7.4.9 Calculation of Finished Hole Size for Through-hole Components

Machine Insertable Component Finished Hole size

Nominal Lead Diameter + 0.014 inch $\leq$ FHS $\leq$ Nominal Lead Diameter + 0.020 inch

Hand Insertable Component Finished Hole size

Nominal Lead Diameter + 0.007 inch FHS Nominal Lead Diameter + 0.020 inch

Select the common finished hole size from **Rule 2-1** that meets the above criteria. When FHS is close to two common finished hole sizes, either:

Round up to larger hole size if there are no other commonly used FHSs on the module, or use hole size to match other commonly used FHSs on the module to minimize PWB drilling costs.

EXAMPLE: THROUGH-HOLE COMPONENT FINISHED HOLE SIZE

Where: Nominal Lead Diameter is 0.022 inch and other PTH components use 0.038 inch Finished Hole Sizes on the module.

Finished Hole size is : between (0.022 + 0.014) and (0.022 + .020)
Therefore, 0.036 $\leq$ FHS $\leq$ 0.042

From Rule 5.5.1:
Acceptable Nominal FHS for this component are:
0.038 inch and 0.042 inch

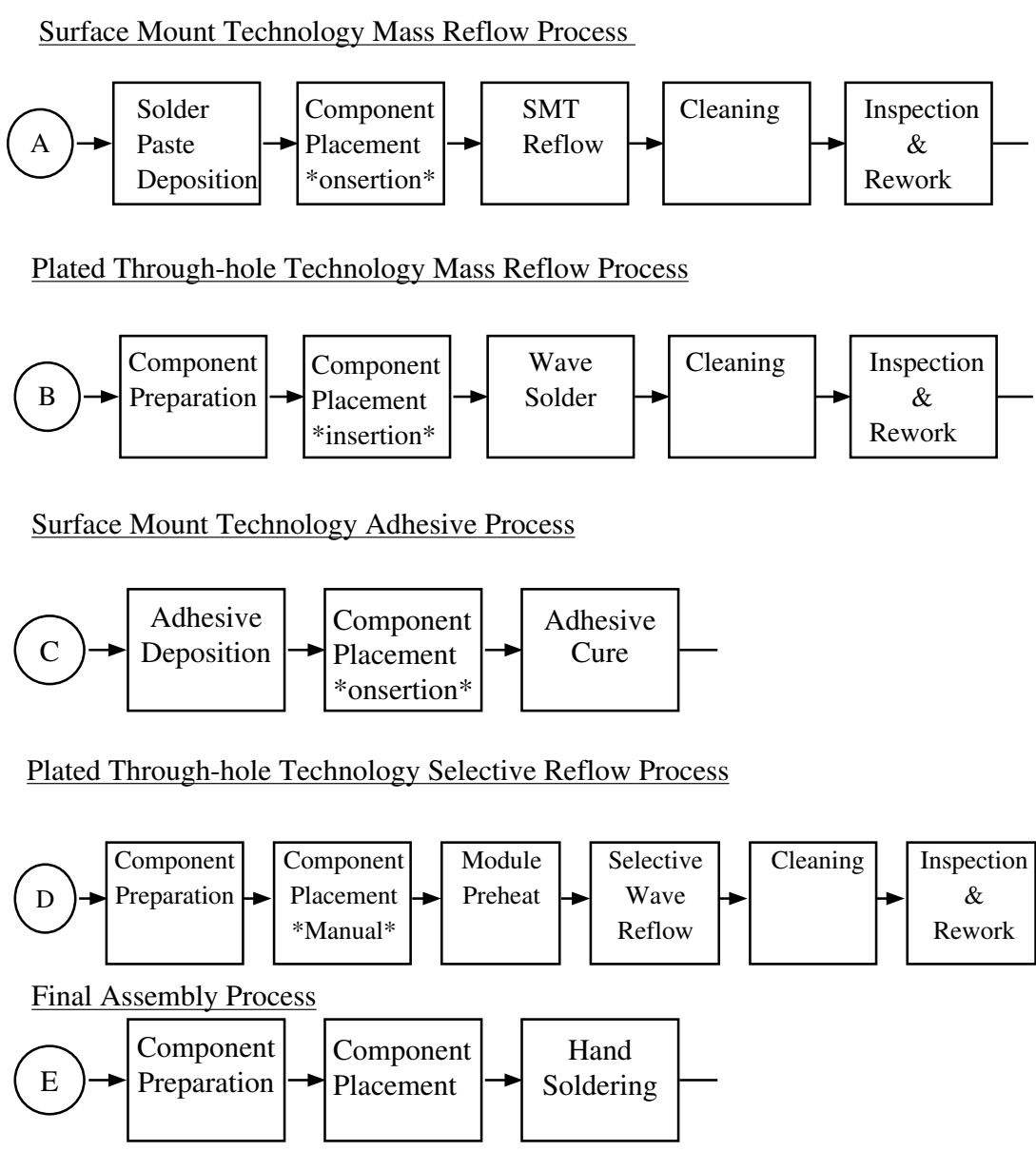
Choose: Finished Hole Size (FHS) of 0.038 inch for this component because other components on this module use 0.038 inch

7.5 Technical Background

7.5.1 Typical Module Assembly Process Flows

Component selection and module layout significantly affect the basic module process flow. Depending on component packaging technology, quantity of components, mix and type of components, along with the module layout, any of the below process flows or combination of flows will be specified. See Figure 7-48. The cost column is supplied **ONLY** for cost trade-off analyses and should not be used to calculate the actual value-added module assembly cost. The process cost represents the minimum cost just to set up and run that particular process. The incremental cost per component is added to that.

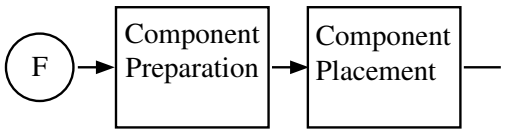
Figure 7-48: Module Assembly Process Flows



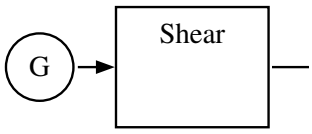
	Cost $	
	Process	per component
A	4.30	0.03
B	1.05	0.12
C	0.25	0.06
D	1.20	0.37
E	0.20	0.86

Module Assembly Process Flows continued:

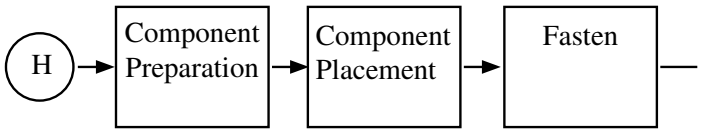
Hand Placement Process



Module Shear Process



Mechanical Assembly Process



Process	Cost $ per component
n/a	0.26
n/a	0.30 per cut edge
n/a	0.26

Example: How to use Figure 46 for a cost **estimate**.

Paradigm (Mixed Mount Module)	Process Elements:	Module Assembly Cost($)
500 SMT components on Side 1	A	4.30 + 0.03 * 500 = 19.30
50 Discrete SMT components on Side 2	C	0.25 + 0.06 * 50 = 3.25
20 Through-hole components on Side 1	B	1.05 + 0.12 * 20 = 3.45
1 Through-hole connector on Side 2	D	1.20 + 0.37 * 1 = 1.57
1 Final Assembled component	E	0.20 + 0.86 * 1 = 1.06
		Total: 28.63

Paradigm (Mixed Mount Module)	Process Elements:	Module Assembly Cost($)
300 SMT components on Side 1	A	4.30 + 0.03 * 300 = 13.30
200 SMT components on Side 2	A	4.30 + 0.03 * 200 = 10.301
1 Through-hole connector on Side 1	D	1.19 + 0.37 * 1 = 1.56
		Total: 25.16

Source of Cost Data: PACE ABC Spreadsheet 6/92 - Normalized labor rate for Digital Manufacturing.

7.5.2 Manufacturing Process Physical Constraints

Table 7-25 details the clearance constraints by process element.

Table 7-25: Process Element Edge Clearance Guidelines

Process Element	Edge Clearance dimensions	Edge Clearance No. of Sides	Component Clearance	Height Restriction Top	Height Restriction Bottom	Height Restriction Side
Solder Deposition	0.175	4				
SMT Placement	0.190	2-Long Edges	0.010	0.400 [1]	0.400	n/a
SMT Reflow[2,3]	0.200	2-Long Edges	TBD	0.750	0.750	1.5
SMT Clean	0.170	2-Long Edges	n/a	n/a	n/a	3.0
Adhesive Dispense	0.200	Shear Edges				
TH Insertion	0.200					
TH Wave[3]	0.200		0.068	2.5	0.375	3.0
Local Wave	n/a		Section 7.6.3	n/a	n/a	
TH Clean				2.0	1.0	3.0
Inspection/Rework	n/a		Figures 15-17			
Shear						
In-Circuit Test			Rule 5-1		Rule 5-4	

[1] A height of 0.400 inch is required for Fuji Placement equipment and 0.600 inch is allowed for Siemens Equipment

[2] Some module assembly reflow equipment requires a 0.400 clearance on the two long edges. Check with Manufacturing Engineering for plant specific requirements.

[3] There is a variety of reflow ovens and wave solder equipment in the company that can accommodate larger component heights.

Notes:

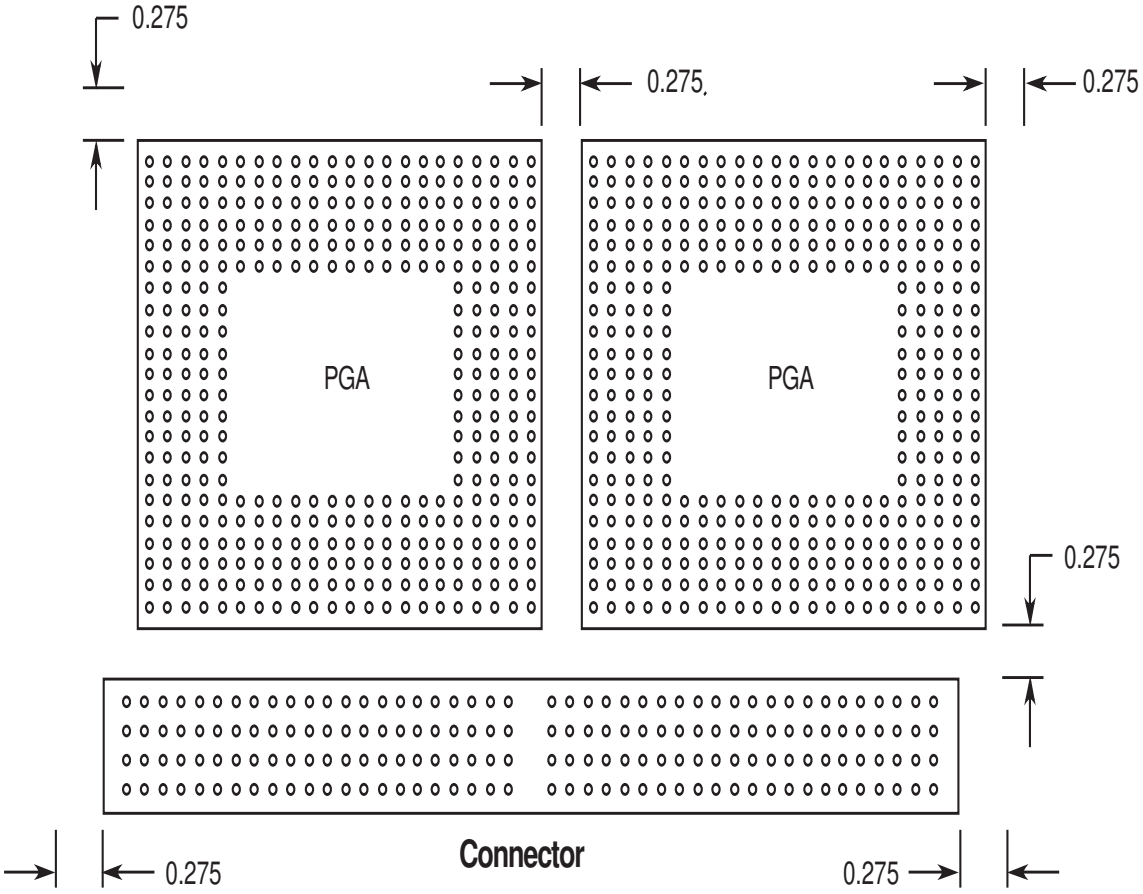
1. The values represented include attached heat sink and component **total** height.
2. These numbers represent only assembly process constraints. Ensure that module test and system specifications are met.

7.5.3 Selective Soldering Guidelines

The preferred through-hole soldering process is the solder wave, however, there are many design choices which require the use of the Selective Solder Process (See **Rule 4-5**). The following guidelines detail specific requirements for the use of the Selective Wave Process. If these guidelines are not followed, the only remaining process option is hand soldering at a cost of $1-$10 per component and an increase in opportunities for defects

Guideline 7 PGA and Connector Clearances

Pin Side of Through-hole Components



Note:

All dimensions are from hole center to hole center and are in inches.

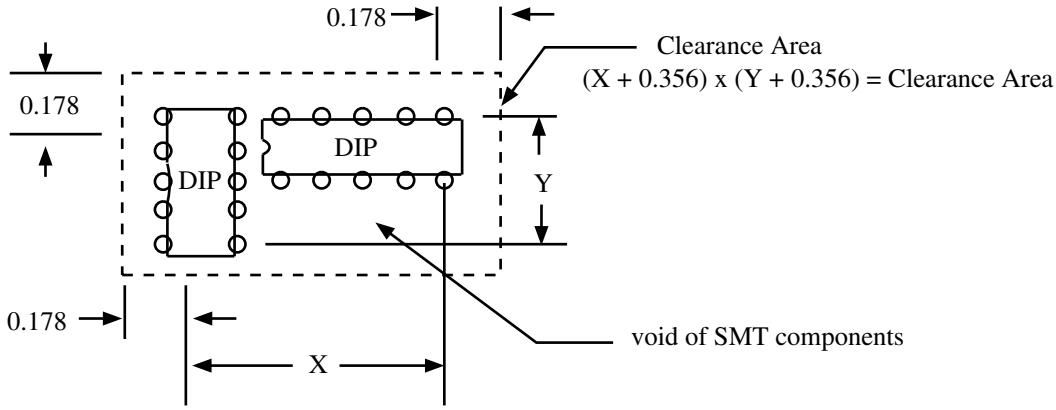
Above dimensions are to keep nozzles independent making them reusable for other products and usable for repair of individual parts.

Guideline 8 PTH Component Grouping

If component PTH pattern locations are closer than 0.250 inch as described in Guideline 1 the following is required because a common nozzle is used for the devices.

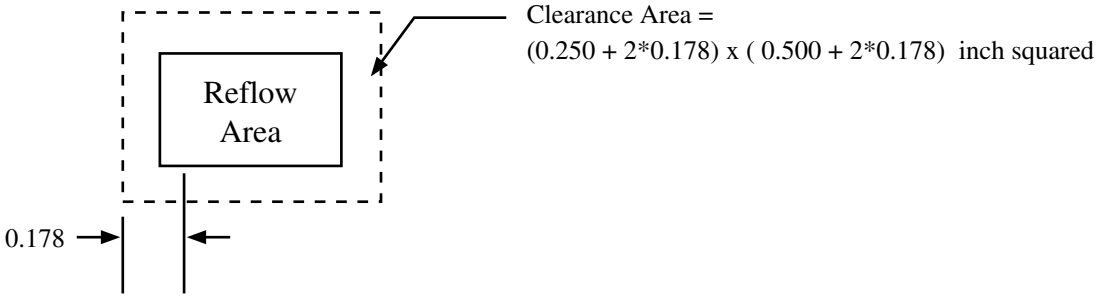
See Guideline 4 if PTH diameter is greater than 0.050 inch.

Example: Two DIPs mounted close to one another - Pin Side



Guideline 9 Minimum Reflow Area (Nozzle Size)

The smallest nozzle size reflow area is 0.250 inch x 0.500 inch.



If the nozzles are reduced in size any further the solder, heat loss is too great and quality level is decreased. See Guideline 4 if PTH diameter is greater than 0.050 inch.

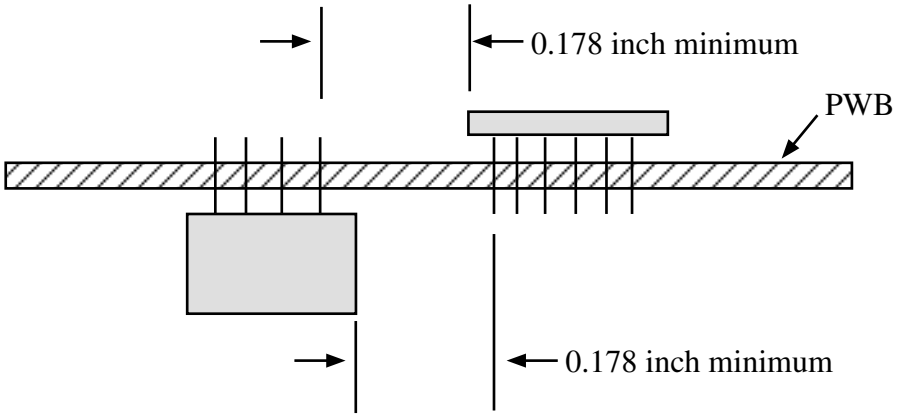
Guideline 10 Clearance for Large Diameter Plated Through-holes

The following table describes the different clearances required by larger size plated through-holed components.

PTH diameter	Pin Side SMT Pad Clearance (inch)
0 ≤ 0.050	0.178
0.051 ≤ 0.100	0.203
0.101 ≤ 0.150	0.228

Guideline 11 Double-sided Through-hole Clearances

The following clearances should be applied when there are through-hole components on both sides of the module.

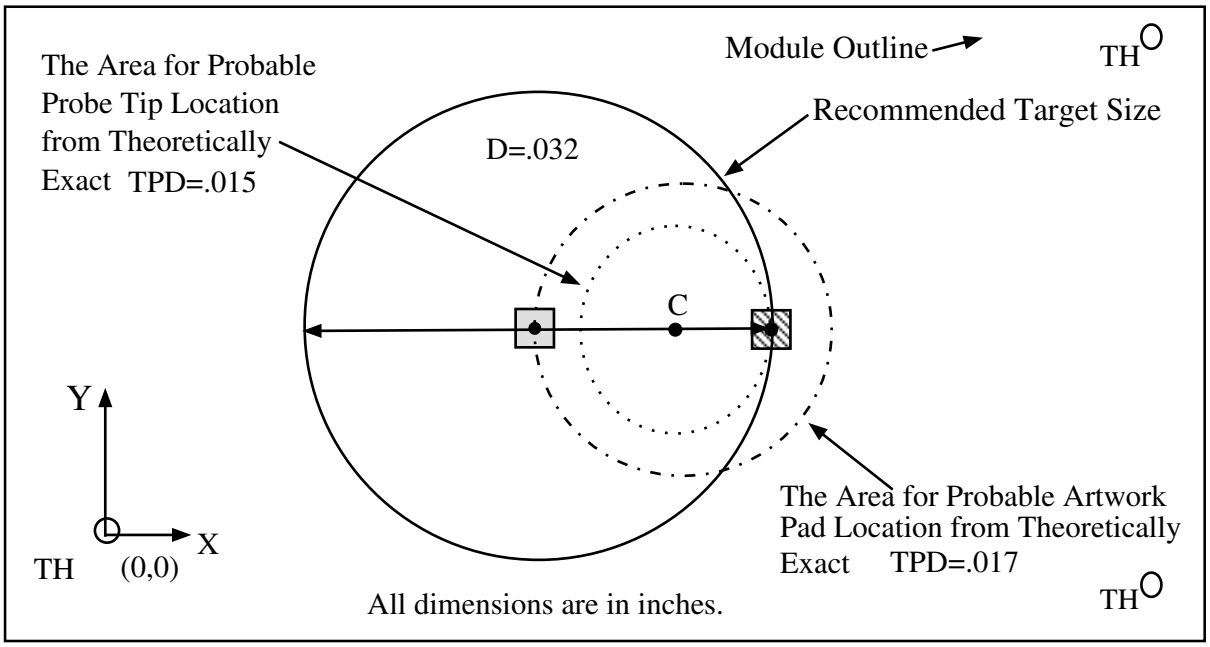


7.5.4 Test Pad Tolerance Analysis

The following tolerance analysis justifies the pad sizes in **Rule 5-1**.

Test pad sizes shall be .035 inch nominal finished size with a tolerance of ±.003 inch (or, alternately stated, minimum manufactured pad size is .032 inch).

Figure 7-49: Test Target Sizing Guide



Assumptions:

1. Tooling holes (TH) are .157 ±.002 inch nonplated through (NPT); tooling hole-to-tooling hole location accuracy = ± .003 inch.

2. PWB pad position mislocation allowance is .017 inch true position diameter.
   (**Note:** See DEC STD 176-04 Surface Mount Printed-Wiring Board Acceptance Criteria, which states that the as-built location of this size target shall be measured from tooling holes identified as TH1 and TH2 in the product data or mechanical drawing.)

3. ATE test fixture probe tip position mislocation allowance is .015 inch true position diameter for up to 15.7 inch x 13.9 inch test area.

4. Single point (that is, cone) probe tip assumed.

7.6 Chapter 7 Review Team

ABO/MEX	Jim Ersfeld
ASO	Dana Duncan
AYR	Hugh Carr
GAO	John Carr
HKO	Wf Yu
KAO	Jerry Benjamin
MLO	Dave Mammone
TAO	
ZGO	
TME	Roy Batchelder
EMT/Chapter Captain	Joanne Mavroides
PWB Chapter Captain	Gerry Gagnon

Chapter 9: Product Data

9.1 The Data Contract

This chapter defines the full menu of product data files that may be supplied to module manufacturing in support the fabrication, assembly and test processes. Each project team, engineering and manufacturing, are responsible to determine the exact *subset* of files from the full menu listing early in the product life cycle that apply to their product. This list of applicable files then becomes the Module Data Document, the data contract for that product.

The set of data files described in the Module Data Document will be provided by engineering for each revision, part and data, and managed by the product team through a data management system for the life of the product.

9.2 Archive Data Structure (ADS)

Today, the design data base is always included in the product data set. The Archive Data Structure (ADS) file has become the internal, proprietary standard for design data bases. Most design tools used within Digital today can write an ADS file, or a converter has been written to perform this translation. Manufacturing has developed many processes and tools based on the ADS file. The investment in these tools will be preserved by migrating the tool input from the ADS file to industry standards over time. Until that migration is complete, the ADS file will continue to be provided. The content of the ADS file is owned by design engineering. The file will be populated with the information required to complete the design. Manufacturing understands and accepts the risks associated with using this file.

9.3 Migration to Industry Standards

The list of files included in this chapter reflect a mix of processes and tools that currently exist in manufacturing and engineering. As these converge into a standard, the list of files will be reduced and migrated to industry standard file formats. For example, the parts list files will converge into a single file with the implementation of the new VAXKPL program. All assembly files will converge into IPC 355 as this file gains acceptance throughout the industry, and the test process activities will migrate towards a single industry standard file. The adoption of commercial CAD tools and the plant partner team will also drive this convergence.

9.4 Product Data

Electronic modules product data is that data generated by design engineering to support the activities of fabricating, assembling, and testing modules within manufacturing. The data will be generic and drive the manufacturing processes regardless of the source of the design or the manufacturer; either function could be external to Digital. Today, the majority of design and manufacturing of electronic modules is expected to remain internal to Digital.

Product data has evolved over the past decade from single data structures containing both engineering and manufacturing data to multiple files which drive specific manufacturing processes. As new technologies were introduced with products, the large data bases could not accommodate the associated data changes in the required time frames. As a result, each project would create a new set of files for their project, usually based on the design tools chosen for that project or the specific equipment in a prime manufacturing plant. Today, there are more than 100 types of files being generated to support modules manufacturing. Many of these will be eliminated by migrating to industry standard files.

Both engineering and manufacturing are moving from fully custom, proprietary CAD/CAM tools to off-the-shelf, externally purchased tools. Several different tools will continue to be utilized based on the users' needs. This shift in business strategy will cause Digital proprietary data sets to migrate to industry standard file definitions.

9.5 Definition of Product Data

Modules manufacturing product data is limited to:

- All the product data required to manufacture the module
- The data created and supplied by design engineering

Product data is not:

- Reference data
- Business data
- Technical and nontechnical data from other recognized Corporate sources (cost, preferred vendor, qualification status, and so forth)
- The raw data that defines how to build a base part number (that is, reference data, base PAL patterns (unblasted), inside the package vendor component information, and so forth)

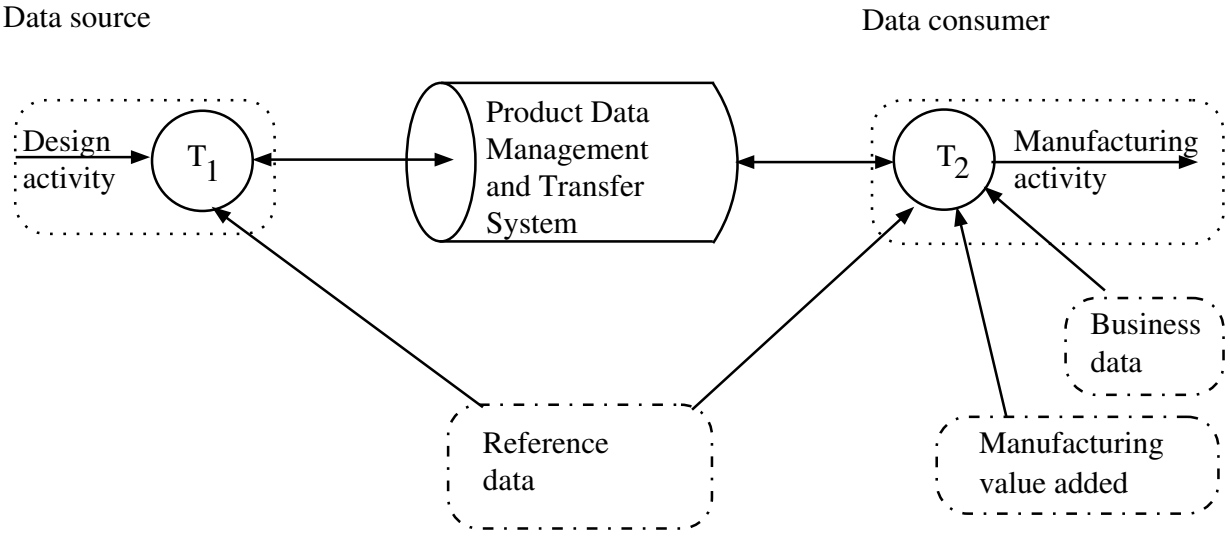
The majority of reference data required to support manufacturing is that information currently found on the SPOC and APPIX system. Further information on these systems, and their associated data element definition and ownership, can be found by contacting John Peachey at SKYHWK::PEACHEY. Reference data will be addressed in greater detail in a future revision of this chapter.

9.6 Concurrent Engineering

Concurrent engineering is best practiced through the early sharing of incomplete knowledge. Partially populated data files should be exchanged by engineering and manufacturing during the development cycle to ensure manufacturability at the time of first prototype build, and that all opportunities are exercised to ensure a competitive product life cycle.

Product data is generic; it attempts to follow the guidelines of *industry standard*s. Today, product data is generated out of translator T_1 in the following figure:

Product Data Flow



The T_1 translator is owned by engineering for the purpose of generating the industry standard files to support the manufacturing operation. The T_2 translator is owned by manufacturing. This step in the process converts the industry standard product data files into the data required to drive the machines on the shop floor of a manufacturing facility. This is also the step in the process where reference data, plant specific data, business data, and manufacturing engineering knowledge is added. The long term goal would be to have the data translators (T_1 and T_2) integrated into the design and manufacturing activity tools. The short term convergence strategy manages the migration of the existing tools to industry standards over the next six quarters.

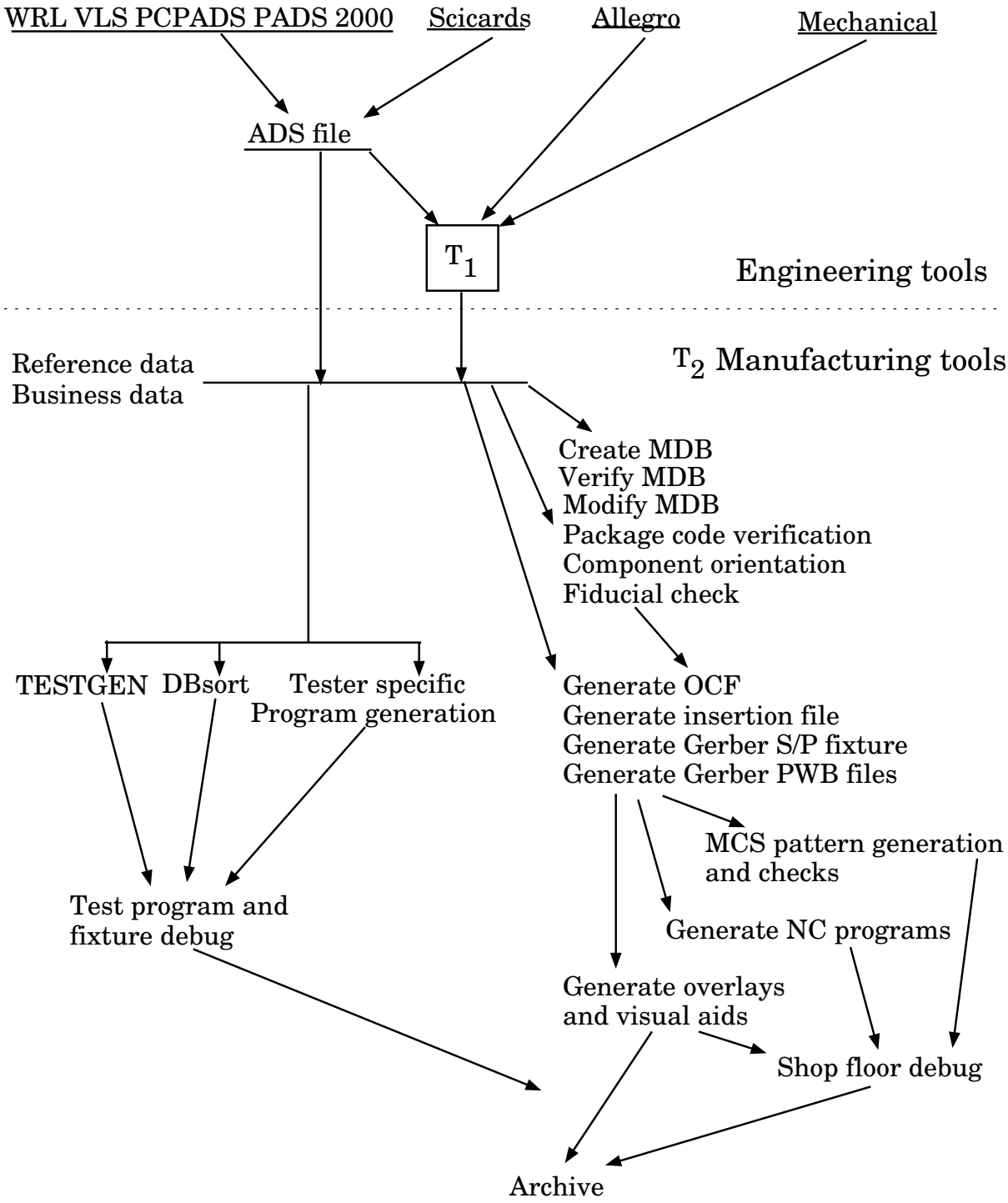
9.7 PDM System

A Product Data Management (PDM) system manages the product data that moves from one site to another. The PDM system provides a common access methodology, defines of the data set for a part revision, conveys the quality of the data set, and establishes the ownership for the data. In addition, it provides timely access to the data from all sites, data set change notification, and lifetime management of the data. The MDA system provides this capability today and is the preferred PDM system within Digital. Documentation on how the product data management process is implemented within MDA is contained under the $INFO part number on the MDA system or by sending a request to MDA::MANAGER.

9.8 Typical Data Flow From Existing CAD Environments

Product data is generated out of many design tools today. The following diagram is intended to illustrate how the product data is utilized within manufacturing. This flow is not specific to any one plant. Each plant has a process specific to their requirements. This diagram is provided for informational purposes only. Specific process questions should to be directed to the plants.

Typical data flow from existing CAD environments



9.9 Industry Standards

Data definitions will attempt to be the recognized, legal *industry standards*.

Data definitions will follow the order of preference when this is not feasible.

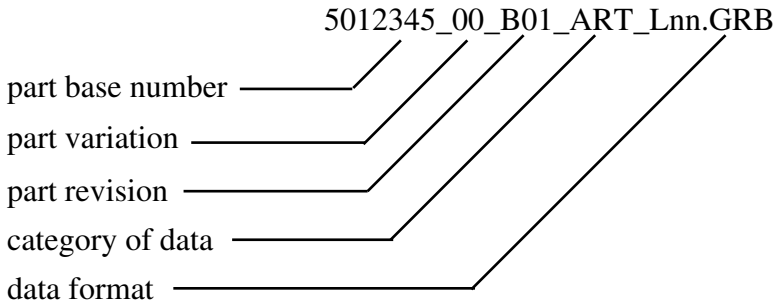
The order of preference is:

Most preferred	De jure standard	} widely used
.	De facto standard	
.	Emerging standard	} not yet widely used
.	Propose as a standard	
Least preferred	Internal only	

9.10 File Naming

Each data or document file is given a unique name chosen to preserve its specific identity. The file names provided in this document are shortened versions of the actual files names to be used. The full and complete file name listings are available in the Master Product Data File document by sending a request to MDA::MANAGER or by logging into your local MDA account and selecting the $INFO part number.

An example of true file naming conventions would be:



9.11 Detailed List of Product Defining Files and Formats for Modules

9.11.1 Data Document

Data document describing which specific files will be generated for a part number. Available on the MDA system under the $INFO part number by typing A-SP-ELENXXX-00-0, or by sending a request to MDA::MANAGER.

9.11.2 Parts Lists

K_PL_DBP_ALL.LST K_PL_DBP_ALL.PLO DES_PART.AKO INC_PART.CMP DES_PART.PLS DES_PART.SPL	Standard VAXKPL output files. See *DEC STD 025-0 Parts Lists*. One PLO sheet required for each LST sheet. The drawing format is controlled by specification EL-MF777-00, *PLO File Specification, Version 3* (in process). ASCII text file used for passing part insertion data to CAM / STREAM software tools in SPL format as defined EK-BATAA-FL*, Formats of DB Sort Input Data Files*.

9.11.3 PWB Reference Data

9.11.3.1 Fabrication

ART_Lnn.GRB	Artwork plot file in ASCII Gerber tenth mil format. Layer L01 = Layer 1 L02 = Layer 2 NM1 = Nomenclature side 1 SM2 = Soldermask side 2 THV1 = Thieving layer side 1
ART_APRDESC.TXT_RPT	Aperture descriptions used for each plot layer in a human readable text file.
ART_HOLE_ALL.EXC	Excellon ASCII drill data format. All indicates the holes go through all layers.
ART_HOLE_Lnn_Lmm.EXC	LnnLmm indicated the holes go through the Lnn and Lmm layers.

9.11.3.2 Test

TEST_CONT.CTF	PWB continuity test program in .CTF format..
TEST_CONT.IPC_356	PWB continuity test program in IPC356 format.

9.11.3.3 Drawing

ARTCHK_LNN.GER or .PS or .PLO	Artwork verification plots in either PLO, PostSript, or Gerber tenth-mil format.
MD & DD	Drawing Directory and Mechanical Drawing in either PLO or PostScript format.

All PWB file specifications are available from the Interconnect Center of Expertise in LJO. Contact Joe Dominick at BOARDS::DOMINICK.

9.11.4 Solder Paste

ART_SPn.GRB	Artwork plot file in ASCII Gerber tenth-mil format. Layer SP1 for side 1 and SP2 for side 2.
ARTCHK_SPn.GER or .PS or .PLO	Artwork verification plots in either PLO, PostScript, or Gerber tenth-mil format.
ART_APRDESC.TXT_RPT	Aperture descriptions used for each plot layer. File is a human readable text file.All Gerber specifications available from the Interconnect Center of Expertise in LJO. Contact Joe Dominick at BOARDS::DOMINICK.

9.11.5 Module Assembly

INS_MAN.PRT	ASCII text report used to assist the preparation of plant specific insertion procedures. Report includes Digital part numbers, reference designators, generic part numbers, and part description. PRT format is defined by the Electronic Design Technology group and is a standard output of VLS. PRT format is defined by the DB-sort documentation, EK-BATAA-FL, *Formats of DB Sort Input Data Files.*
ONS.OCF	Onsertion data file. Common OCF format specification containing the physical component information required to drive the onsertion process. See EK-BAVAA-FL, *Onsertion Data File.*
INS_MAN.PLO	Graphic aid for the preparation of manual insertion procedures. Unit Assembly Drawing of the module and its parts (including reference designators and Digital part numbers) in PLO format.
MAAPP input file	ASCII file containing the information required to drive the MAAPP process (assembly and visual aids). This file is curently generated only out of the Allegro design system and is subject to change as development continues. For further details contact AISG::FRASER.
WRL_PLACE.PKG	WRL output file describing the physical characteristics on the board. See EK-BASAA-FL, *A Basic Introduction to WRL Tools.*

9.11.6 Module test

ICT_NET.NET	Network data ordered by network; in NET format as defined by the DB-sort documentation, EK-BATAA-FL, *Formats of DB Sort Files.*
ICT_PART.DPL	Detailed device level data applicable to in-circuit test as defined by DB-sort documentation, EK-BATAA-FL, *Formats of DB Sort Files.*

ICT_PART.PRT	Part data report. Report includes Digital part numbers, reference designators, generic part numbers, and part description. The format is defined by the Electronic Design Technology group and is a standard output of VLS. The format is defined by DBsort documentation, EK-BATAA-FL, *Formats of DB Sort Files.*
GR.CKT	Genrad 227x circuit description (netlist) file as created by Genrad translators out of the Allegro design system. See EK-BATAA-FL, *formats of DB sort files*.
XREF.DAT	Global signal cross reference for a complete design; with local and global part cross reference. VALID PSTXREF.DAT format. See EL-EN432-00, *Archive Data File Specification.*
NET_LST.XREF	Netlist cross reference data extracted from Allegro using the GenXref program. Contact ECADJR::INCORVAIA for further information on the Allegro design system.
TEST_LOG.TXT_RPT	Allegro testprep log file with the X,Y location of the testpoints, vias, pins, and reference designators in the format as generated from the Allegro design system. Contact ECADJR::INCORVAIA for further information on the Allegro design system.
TEST_PROBE.EXC	Location of test probe drill points in Excellon II drill format. Specification available from the Interconnect Center of Expertise in LJO. Contact Joe Dominick at BOARDS::DOMINICK.
DIAGNOSTICS	As required
Grandfathered WRL tool files	See EK-BASAA-FL, *Basic Introduction to WRL Tools.*
WRL_STRUNGWR.TXT_RPT	Strung wires net listing and component location information in an ASCII file.
WRL_HIARC.TAR_Z	Compressed collection WRL implementations and interface files.
WRL_LREF.TXT_RPT	Cross reference file of signal names and node connections.
WRL_UNTENT.BIN	Binary output of WRL router containing physical etch and pad description.
WRL_PCB.TXT_RPT	WRL PCB file that describes the physical characteristics of the PC board.

9.11.7 Customization of Programmables

All programmable files referenced in *DEC STD 184-0 Programmable Integrated Circuit Documentation: Process and Requirements.*

9.11.7.1 PALASM

PLT.TXT_RPT	PAL fuse plot in PLT format specified by PALASM.
FPLS_PLT.TXT_RPT	PAL sequencer fuse plot in PLT format specified by PALASM.
ROM_PLT.EXE	Binary source file to blast ROMs in PLT format specified by PALASM.
JDC.TXT_RPT	JEDEC format blaster file in JEDEC format.
FPLS_JDC.TXT_RPT	JEDEC format blaster sequencer file in JEDEC format.
PAL.TXT_RPT	PAL ASCII source file used for the PLT and JDC files.
LIS.TXT_RPT	Sequencer ASCII source files used for the PLT and JDC files.

9.11.7.2 CUPL

DOC.TXT_RPT	PAL fuse plot for the entire fuse table specified by CUPL "f" output file.
FPLS_DOC.TXT_RPT	PAL sequencer fuse plot specified by the CUPL "f" output file.
JED.TXT_RPT	JEDEC format blaster file in JEDEC standard format created by CUPL "j" output file.
FPLS_JED.TXT_RPT	JEDEC sequencer blaster file in JEDEC standard format created by CUPL "j" output file.
PLD.TXT_RPT	PAL ASCII source file used to generate the .DOC and .JED file.
ROM.EXE	ROM JEDEC blaster file in binary executable format as generated by ROMGEN.

9.11.7.3 PROM

FLASH_HEX.TXT_RPT	ASCII HEX file used to blast flash PROMs in Intel format.
FLASH_SREC.TXT_RPTASCII	SREC file used to blast SROMS.
UV_HEX.TXT_RPT	ASCII HEX file used to program UV PROMs in Intel format.
DES_PART.KRM	Revision matrix.

All programmable files are referenced in *DEC STD 184-0 Programmable Integrated Circuit Documentation: Process and Requirements.*

9.11.8 Change Control

PCA_nnn.TXT_RPT
ECO_nnn.TXT_RPT
ECR_nnn.TXT_RPT

These are change control documents. nnn is the PCA or ECO file revision. Refer to *DEC STD-100-5 Engineering Change Orders - Financing ECOs to Hardware.*

Regenerate the appropriate data files listed above to produce a complete and managed data set.

9.11.9 Inspection and Visual Aid Drawings

This category of files includes Unit Assembly (UA), Circuit Schematic (CS), Block Diagram (BD), Drawing Directory (DD) and Timing Diagram (TD). In PLO, PS, HPGL, Versatec, or ASCII text format as appropriate.

9.11.10 Design Data Bases

MODULE.ADS — Complete physical design data for the module. in ASCII ADS format as defined by the Electronics Design Technology organization. See EL-EN432-00, *Archive Data File Specification.* Many assembly and test tools utilize this file as *the* major source of product data.

MODULE.BRD — Complete physical design data for the modules in binary BRD format as defined by the Allegro system. Specification available from Cadence Corporation, or contact A.J. Incorvaia in the ECAD organization in MLO, ECADJR::INCORVAIA.

Chapter 11: Module Electrical Design

Higher data rates and faster signal risetimes mean that the physical configuration of the signal interconnect has a larger effect on the characteristics of the signals and on the resulting electrical performance. This chapter briefly describes the significant electrical effects, and provides data, guidelines, and general methods that may be applied to assure good electrical performance. The focus of this chapter is on CMOS and TTL based systems.

11.1 Overview

This section shows a few examples of signal and noise problems that can be caused by the electrical characteristics of interconnect.

11.1.1 Simultaneous Switching Noise

Simultaneous switching noise is an ac voltage generated across the impedance of the power distribution interconnect when an integrated circuit (IC) draws transient currents during switching. Faster signal risetimes and wider busses cause larger transient currents and more noise. Switching noise may be generated by any portion of the power interconnect between the supply and the ICs.

Simultaneous switching noise is of concern for two basic reasons.

- A chip may not be able to switch effectively if the supply voltages are not fully recovered from the previous switching event.
- The reference voltage of input circuits will be shifted by the noise that is generated, potentially causing logic errors.

Simultaneous switching noise may result in either long-term effects, where the average supply voltage at the chip droops, or short-term effects, where the voltage oscillates (rings) for a period of time after a switching event.

The following figures show examples of switching noise generated by the inductive characteristics of an IC package. Figure 11-1 shows a simple but useful model of the situation. There are a number of output (pin) drivers switching together on a CMOS-2 chip in a multilayer ceramic package. Figure 11-2 shows the collapse of the supply voltage $(V_{dd} - V_{ss})$ at the IC. The initial, negative pulse, if large enough, can significantly affect performance.

Figure 11-3 shows the resulting distortion of an output signal that is switching. Figure 11-4 shows the effect of the inductance in the reference paths that are shared between switching and quiet outputs. (Note that these waveforms are at the driving device, waveforms at receivers are probably different) The switching activity generates noise on the references, which also appears on an output signal that is inactive. Similar noise could be generated on an input signal that shared the same references.

Figure 11-1: Simple Schematic for Simultaneous Switching Noise

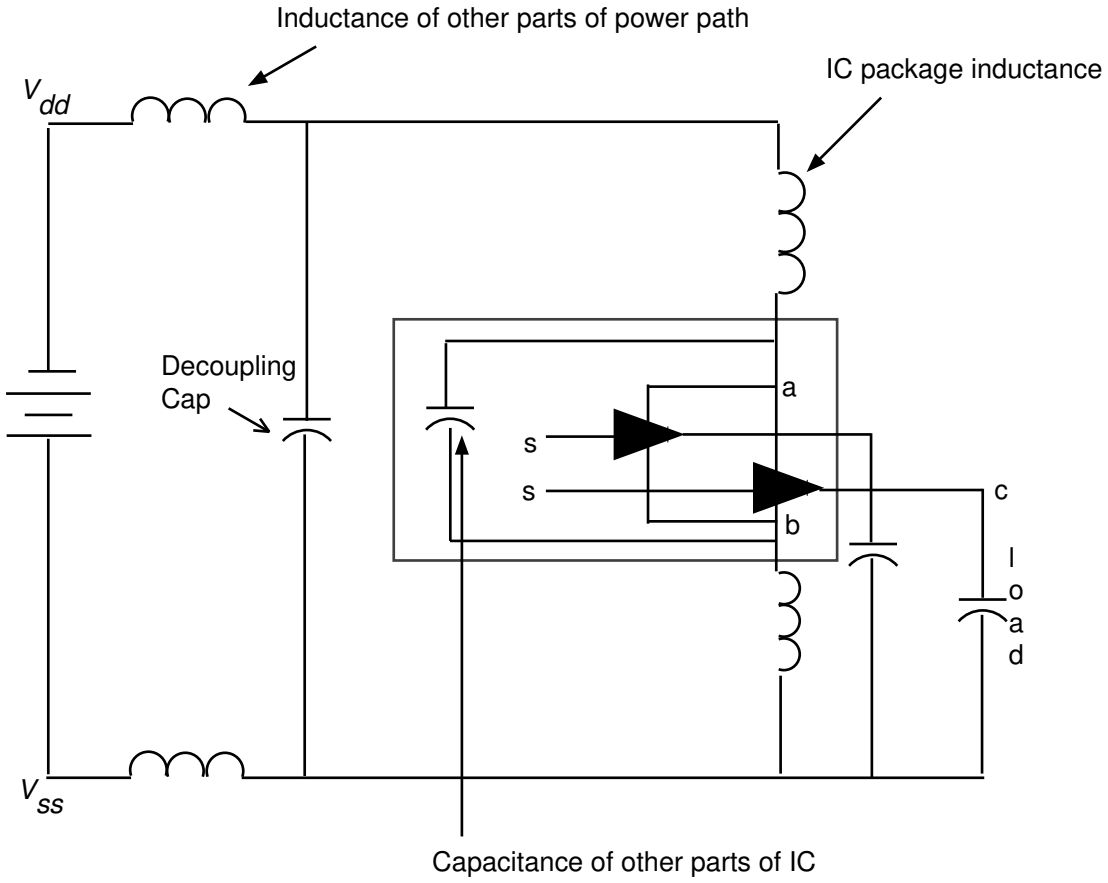


Figure 11-2: Measured Supply Voltage (V_{dd}-V_{ss}) On-Chip

Figure 11-3: Active Output Signal at Chip

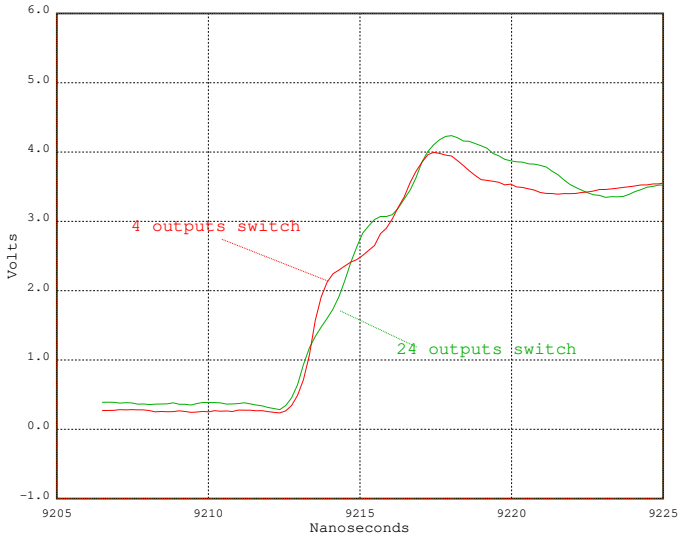
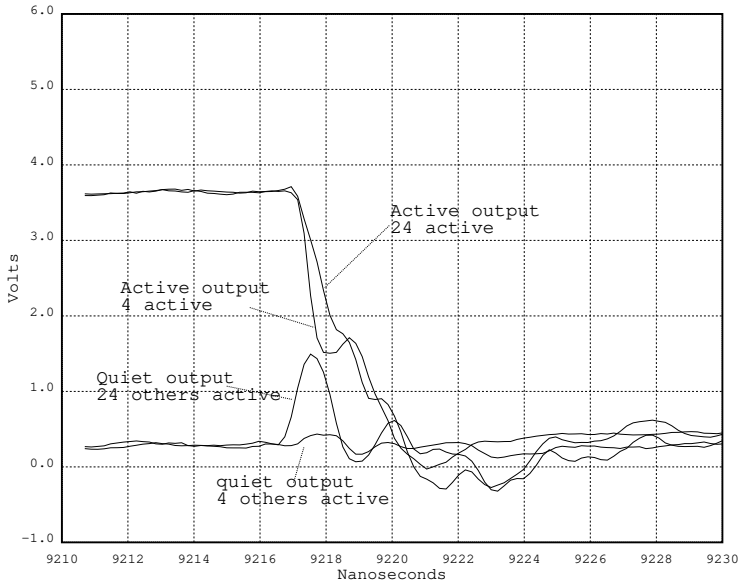


Figure 11-4: Inactive Output Signal at Chip

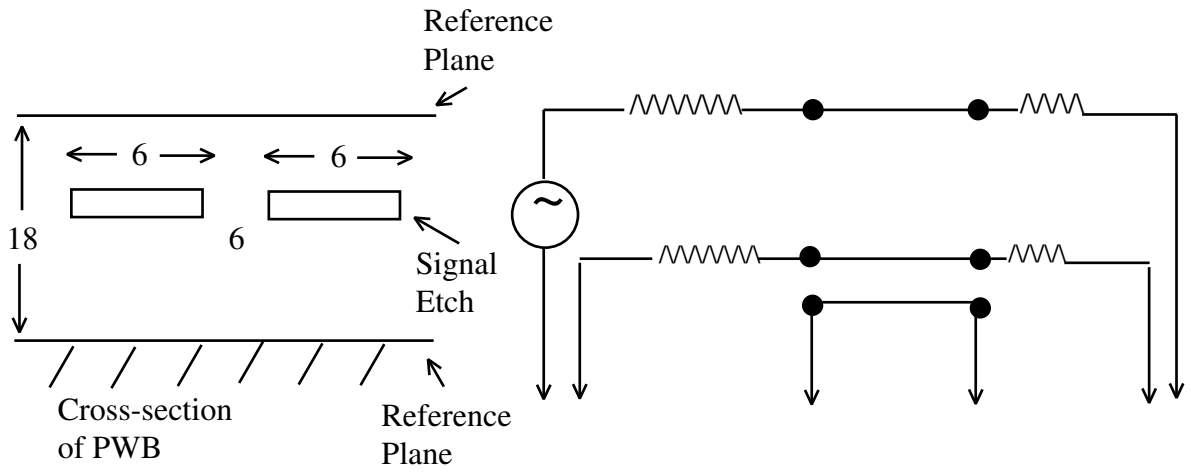


11.1.2 Crosstalk

Crosstalk is the result of distributed capacitive and inductive coupling between neighboring signal lines. Crosstalk from neighboring lines causes noise pulses that can lead to false triggering or timing errors in a receiving device. Because the timing relationship between the signals on adjacent lines may not be known, it is not always possible to predict when crosstalk will occur. In the case of a bus, where all signals in a group are active simultaneously, the effective characteristics of the lines will vary depending on how many lines are switching, and in what relative direction.

Figure 11-5 shows a typical coupled transmission line situation, and figure 11-6 shows the resulting crosstalk waveforms, simulated using the Simulation Program with Integrated Circuit Emphasis (SPICE). The effect of the coupling between signal paths can be seen. The signal that is switching (the culprit) is distorted slightly by the coupling. The signal that is “quiet” (the victim) shows noise pulses at both ends. The amplitude, duration, and timing of the pulses depends on the characteristics of the lines and on the risetime of the culprit signal.

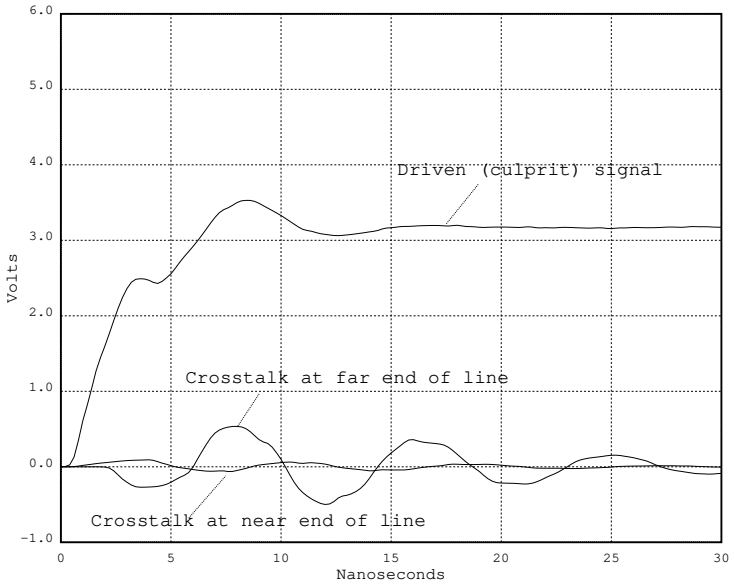
Figure 11-5: Typical Coupled-line Configuration



Note that the crosstalk waveforms are different at the two ends of the line. Whether or not crosstalk is a problem will depend on the pulse amplitude, duration, and arrival time at the receiving device(s). In general, for a receiver to respond to a crosstalk pulse, its input threshold must be crossed for a sufficiently long time, at a time when it is being enabled or clocked,or is otherwise susceptible to noise. Note also that these waveforms will be distorted by any loading or impedance changes in the lines.

Crosstalk-like noise may also be generated by an impedance in a return path that is shared by two or more signals.

Figure 11-6: Simulated Crosstalk Pulses: 1 Victim, 1 Culprit



11.1.3 Transmission Line Effects

At sufficiently fast edge rates, signal interconnect behaves as transmission lines and the effects of the signal propagation velocity along the line and the characteristic impedance of the line become significant. The following conditions may have to be considered.

- Additional time delay because of the interconnect
- Voltage division between driver and line or between lines different impedance
- Reflections from impedance changes, such as loads and connectors
- Overshoot and ringing of signals at inputs

The following figures show examples of how signal waveforms may be affected in a typical case.

Figure 11-7 shows an example of a transition where the voltage plateaus for a time. This is caused by the interaction between the transmission line impedance and the driving and receiving device's output and input impedances. If a plateau is present too long between logic levels, an additional time delay may be incurred, or receiving devices may become unstable. Plateau voltage is controlled by the driver output current and the transmission line effective impedance. Plateau duration is controlled by the length and configuration of the transmission line network.

Figure 11-7: Plateau Caused by Voltage Division

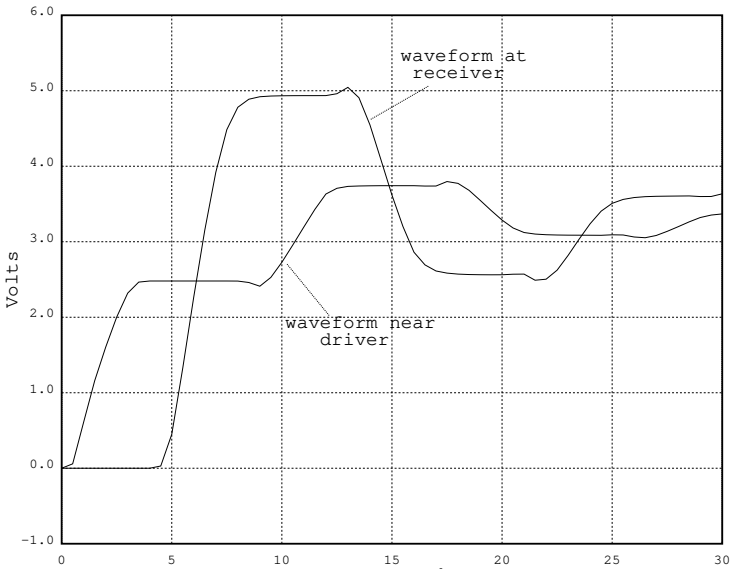
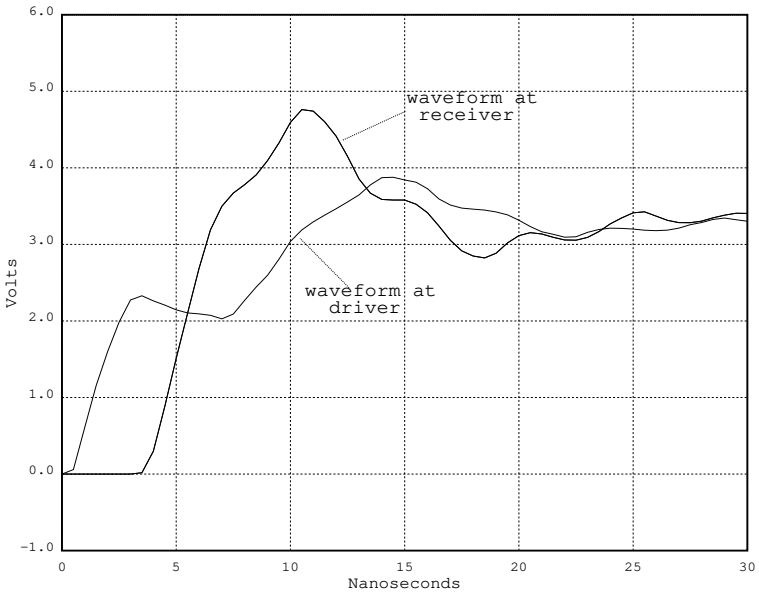


Figure 11-8 shows an example of a signal that has a reflection from a branch in the network. If this reflection is large enough, timing errors or false triggering can occur. Similar reflections are caused by loads, stubs, and connectors.

Similar reflections may be caused by discontinuities in the signal's return path. Such a discontinuity may be introduced by a connector, where the reference pins are not near the associated signal.

Figure 11-8: Reflection from Impedance Change



11.2 Definitions

This section contains definitions of symbols and names used in this chapter and that are commonly used in general signal integrity work.

11.2.1 Signal Quality Metrics and Interconnect Parameters

1.

$$t_{pd} = \sqrt{L_0 C_0}$$

The signal propagation time per unit length in a uniform, lossless transmission line. The total propagation delay will be (line length) x t_{pd}. For microstrip on FR-4, t_{pd} is approximately 0.15 ns/inch; for stripline in FR-4 it is approximately 0.18 ns/inch.

2.

$$t'_{pd} = \sqrt{L_0(C_0 + C_{load})}$$

The signal propagation time per unit length in a uniform, lossless transmission line with load capacitance C_{load} per unit length, uniformly distributed.

3.

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

The characteristic impedance of a uniform, lossless transmission line.

4.

$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_{load}}}$$

The characteristic impedance of a uniform, lossless transmission line with load capacitance C_{load} per unit length, uniformly distributed.

5.

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

The voltage reflection coefficient between impedances Z2 and Z1. This is the ratio of the reflected voltage to the incident voltage.

6. Rise and fall time, t_r, t_f
   Time required for signal at a specified point to move through a transition. In this document, it is from 10 to 90% of the final value.

7. Line delay, t_d
   Time required for a signal to travel from driver output to specified receiver input. Rise and fall time and reflection effects are not included, so this is t*ime of flight.*

8. Settling time, t_s
   Time required (after t_d) for signal to stay within a specified amount of its final value. Amount may be determined by logic thresholds or by other noise margin considerations.

9. Total delay, t_t
   Total delay from driver to receiver, $t_d + t_s + t_r$ (Include input loading effect if appropriate) The maximum or minimum acceptable t_t is determined by system timing requirements.

10. Overshoot voltage V_{ov}
    Amount by which signal passes its final value during a transition. Excess overshoot (in either direction) can cause a receiving device to exceed its timing specifications or to malfunction in some other way.

11. Timing skew, δt
    Difference in time delay between related signals. Depending on the case, it can include any or all of variations in driver output delay, line length, loading, driver risetime, and receiver thresholds and interconnect impedance variations. The maximum tolerable skew is determined by system timing requirements and the need to maintain synchronization.

12. Noise margin
    Minimum difference between the steady state voltage of a signal and either the nearest threshold voltage or nearest absolute maximum or minimum input voltage of any device driven by that signal.

11.2.2 Signal Functions

It is useful to classify signal lines according to their sensitivity to noise and their importance to system operation. This section describes the various signal function.

1. Clock Signals
   A small number of signals that serve to synchronize some portion of system activity. Clock signals are generally required to have the following characteristics.

   a. Transitions clean and uniform

   b. Skew between clock signals controlled. In general, the earliest and latest clock arrival times are interesting events, while the nominal arrival time is not.

   c. Overshoot and ringing controlled so that $t_s \sim O$

d. t_r and t_f within limits set by skew considerations and receiver input requirements

e. Noise from other sources (crosstalk, for instance) limited to a small fraction of signal swing.

f. Adequate dc noise margin maintained at all times.

2. Asynchronous Control Signals
A small number of signals whose transitions are used to control system activity in some way. That is, they are received by edge-sensitive devices. For instance, these are the signals that control the latching of data into a chip. Asynchronous control signals are generally required to have the following characteristics.

a. Transitions monotonic

b. Overshoot and ringing controlled so that $t_s \sim 0$

c. t_d known and controlled so that the required timing relationships between signals can be maintained.

d. t_r and t_f within specified limits.

e. Adequate dc noise margin maintained at all times.

3. Data, Address, and Control signals
Signals that are sampled or latched at a known time. One source and one or more receivers. Data, Address, and Control signals are generally required to have the following characteristics.

a. $t_d + t_s$ less than a limit set by system timing requirements. Usually there is a time interval, relative to a clock signal, when data on the bus must be valid (settled).

b. Overshoot less than a limit set by the characteristics of the receiving devices.

c. Adequate dc noise margin maintained during the appropriate sample or latch intervals.

4. Busses
Multiple driver/receiver pairs tied together on module or between modules or between backplanes, and so forth. Usually large number of bits. For instance, RDAL, XMI, SCSI. May be synchronous or asynchronous. Bus signals are generally required to have the following characteristics.

a. $t_d + t_s$ less than a limit set by system timing requirements. Usually there is a time interval, relative to a clock signal, when data on the bus must be valid (settled). All lines in the bus must be settled.

b. Overshoot less than a limit set by the characteristics of the receiving devices.

c. Adequate dc noise margin maintained during the appropriate sample or latch intervals.

5. Reset and Power-Clear Signals
   A small number of system or module level status/control signals. Normally quiescent. One source, many receivers. These should be treated in the same way as clock signals. Noise on reset signals can be a real problem.

6. Cables and Connectors
   Signal cables and their associated connectors that stay within an enclosure. May connect two or more modules in a backplane, or may connect a module to one or more devices (within the same enclosure), for instance a disk drive to its controller. Required signal characteristics will depend on the type of signals being carried.

7. I/O
   Signals that enter or leave the enclosure. I/O can be either multiple signals (a bus) or a single signal (a serial line). Required signal characteristics will depend on the type of signals being carried. I/O often involves cables and connectors.

11.2.3 Network Types

1. Point to point
   One driver, one load. Easy to control signal quality.

2. Point to *lump* or far-end cluster
   One driver, a number *N* of loads some distance from the driver but all within a short distance of each other. If the delay between receivers is less than $t_r/4$, (that is, $lt_{pd} > t_r/4$), they appear to be a load of *N* times the value at the end of the transmission line. Signals tend to be quite clean at the receivers, but may have increased risetime because of the larger capacitance present, $t_r \sim 2.2\ Z_0\ C_{load}$. Near the driver, the signal will show a large negative reflection from the load.

3. Star
   A number *N* loads connected to one driver by individual lines. (one load per line) The lines should be the same length, within about 1/8 risetime. Signals are clean if the driver output current is adequate, in general, $R_{driver} < Z_0/N$. The signal near the driver will be distorted.

4. Multiload
   A number *N* loads distributed along a line from the driver. The loads are within 1/10 risetime of the "main" line. If the stubs are less than $t_r/4t_{pd}$ from each other, they may be treated as uniformly distributed along the line. In this case, the line will behave as if its impedance and delay include the added C per unit length. Note that there will likely be a portion of the line without loads, and a portion with loads. These sections will have different effective impedances (Z_0 and Z'), and so there will be an impedance mismatch between them. The propagation delay will be different in the two sections as well.

5. Multibranch
   Similar to multiload, but the loads are farther from the main line. As that distance increases, the connecting lines may be treated as additional load capacitance, then as transmission lines. When the connecting lines are long, signal behavior on this network may be complex, and it is not possible to terminate this network such that there will be no reflections.

   Note that the multiload and multibranch transmission line networks, with their distributed loading, show low-pass filter characteristics when the loads are uniformly spaced. This can be a problem, for instance, in a backplane bus application. Analysis of typical backplane configurations has shown the presence of stopbands starting as low as 400 MHz. See *Physical Limitations of Backplane Busses on Signal Integrity,* by Michael Tsuk, for details.

6. Multitrunk
   A combination of star and multi-trunk, that is, can have branch points anywhere. Signal behavior is complex, it is not possible to terminate this network such that there are no reflections.

11.2.4 Termination

These are the commonly used termination schemes.

- Series
  A resistance R_s is added at the driver, so that the total source impedance, $R_s + R_{dr}$, matches the impedance of the transmission line. This may be a resistor mounted on the printed-wiring board (PWB), or may be built into the driver IC. The signal swing into the line is

$$V_{signal} = V_0 \frac{Z_0}{R_{dr}+R_s+Z_0}$$

  There is a reflection from the far end of the line, which is open ($\rho \sim 1$), so the voltage approximately doubles there. This reflection travels back toward the driver and is absorbed, and the line is settled in one round-trip time. Input thresholds are generally not crossed until the reflected (backward-traveling) signal arrives, so the receiver at the far end of the line switches before any receivers near the driver. The following table shows recommended initial values for the resistance for each type network.

Table 11-1: Series Termination

Network	$R_t + R_{dr}$
Point-to-point	Z_0
Point-to-lump	Z_0
Star	Z_0/N
Multiload	Z_0 Z'_0 if loads within tr/4 of driver
Multibranch *	Z_0 Z'_0 if loads within tr/4 of driver Network
Multitrunk *	Z_0 Z'_0 if loads within tr/4 of driver

(*) These networks cannot be perfectly terminated

Note that R_{dr} is dynamic during switching, so the resistance value of the "on" transistor should be used.

Series termination can have a number of other good effects, including reducing the power dissipation in a CMOS IC, reducing simultaneous switching noise by reducing the magnitude of the transient currents when the output drivers switch, and reducing crosstalk by reducing the amplitude of the initial voltage step driven into the line.
The driver must be able to both source and sink current, that is, actively drive both high and

low.

- Diode (diode clamp)
  A fast (low capacitance, inductance, and resistance) diode is connected from the end of the line farthest from the driver to either V_{dd} or V_{ss} , and limits the overshoot there by clamping to the reference voltage. The diode must be placed close to the receiver. Two diodes are often used, so that overshoot in both directions will be controlled. The HP2822 or similar diodes are suitable, and are packaged in pairs. Notice that when the diode turns on, the line is approximately shorted to reference, which causes a reflection until the voltage changes enough to turn the diode off. Simulation may be needed to verify diode performance because of this. Power dissipation in the driver is increased compared to series termination. A good model of the diode(s) will be required. Note that many standard IC's have input protection diodes that perform the same function.

The driver must be able to both source and sink current, that is, actively drive both high and low.

- Parallel dc
  A resistance R_t is connected from the end of the line farthest from the driver to a voltage reference V_t. The value of R_t normally matches the line impedance, so there is no reflection ($\rho=0$). V_t is chosen considering both dc levels and transient performance. This termination is often implemented with a resistor from the signal to V_{dd} and another from the signal to V_{ss}, avoiding the problem of bringing another voltage (V_t) onto the board. Resistor values are constrained by
  * Desire to match the Z_0 of the line
  * The high and low output currents of the driver
  * The desired high and low input voltages to the receivers
  * The current flowing from V_{dd} to V_{ss} through the terminating resistor pairs.
    Values for R_1 and R_2 may be calculated from driver output currents and desired input voltages according to the following:

$$R_1 = \frac{V_{dd}\left(1-\frac{V_L}{V_H}\right)}{I_{OL}+\frac{V_L}{V_H}I_{OH}}$$

$$R_2 = R_1\frac{V_L+\frac{I_{OL}}{I_{OH}}V_H}{V_{dd}-V_L+\frac{I_{OL}}{I_{OH}}(V_{dd}-V_H)}$$

I_{OH} and I_{OL} are the driver output high and low currents
V_H and V_L are the desired high and low voltage levels
V_{dd} and V_{ss} are the high and low supply voltages

In addition to this, the Thevenin resistance,

$$R_t = \frac{R_1 R_2}{R_1 + R_2}$$

should be close to the impedance shown in the following table.

The current through the terminator,

$$I = \frac{V_{dd}}{R_1 + R_2}$$

should be acceptably small. Remember that there may be may copies of this terminator in parallel on a module.

Table 11-2: Parallel DC Termination

Network	R_t
Point-to-point	Z_0
Point-to-lump	Z_0 placed at branching point
Star	not recommended, load too heavy
Multiload	Z'_o
Multibranch *	Z'_o
Multitrunk *	Z'_o

- (*) These networks cannot be terminated perfectly

- Parallel ac
  Similar to parallel dc, but with a capacitance added in series with R_t to break the dc path. The capacitor value must be large enough that it has low impedance at the expected edge rates, but that is small enough to charge/discharge quickly and not adversely affect the edge rate. The 10 to 90% charging time of the capacitor is $T=2.2RC$, so we can calculate the maximum usable value of C_t for a maximum acceptable T (typically two or three times the signal risetime)

  $$C_t = \frac{T}{2.2R_t}$$

  See Table 11-2 for initial resistance values. The driver must be able to both source and sink current, that is, actively drive both high and low.

11.3 Design Guidelines

This section contains methods, suggestions, and data, which may be applied to avoid or correct many electrical problems.

11.3.1 General Guidelines

- *Ground* is a misleading term, implying the existence of a fixed, 0-volt reference. Such a reference does not exist.
- Use the slowest acceptable risetime and data rates -- all transmission line effects and potential EMI problems will be reduced.
- Keep signal paths short -- transmission line effects and potential EMI problems will be reduced. A good placement of components can do much to keep line lengths down.
- Use point-to-point connections -- simpler networks have simpler, more predictable behavior.
- Consider power distribution early in the design effort.
- Keep IC families grouped together, that is, keep chips with different voltage swings and speeds apart.
- Keep signals with different functions and different time dependencies away from each other -- for instance, keep clocks away from asynchronous control, away from data/address/control.
- Terminate signals (especially long ones) to control reflections and standing waves, to improve signal quality and reduce radiation.
- Design for Z_0 $\pm 15\%$ on the PWB, if possible, to reduce manufacturing process tolerance problems and cost.
- Maintain small current loops in signal paths -- that is, the return side of the loop stays close to the signal side.
- In general, signals are less affected by additional lead length than is power and logic reference. Where a choice is to be made, it is often better to route power and reference through the shorter leads of a connector or package.
- Avoid dispersion etch between surface mount pads for decoupling capacitors or terminating resistors and the vias that connect to the reference plane. The etch adds undesirable inductance in the reference path.
- Place the fastest chip close to the stable supply (for instance, the local regulator).

- Avoid sharp right angle turns in signal etch.
- The input protection circuits in many standard ICs provide good clamping of overshoot without adding additional parts. **Note:** This is not always the case.
- Series terminating resistors may be put on-chip, if the variation in value caused by the IC process and the increased power consumption are acceptable.
- Use power and reference planes in PWBs.

11.3.2 EMI Control

- Keep all signal paths as short as possible.
- Keep the rise/fall time as slow as possible. Always consider the impedance of a signal path and the return path. Find the RF voltage from the intended current through this impedance. Keep this RF voltage as low as possible by lowering the impedance or the current. At frequencies of 100 MHz and above, 100 uvolts is a significant RF voltage!
- Keep high speed (fast rise/fall time) signals physically separated from low speed signal lines and I/O lines as much as possible.
- Keep all microstrip and strip line signal paths away from the edge of the reference plane (by at least 0.25")
- Use strip line configuration whenever possible for high speed signals. High speed signals (fast rise/fall times) should not be routed on many different layers. Keep the distribution of these signals simple.
- Avoid any break in the reference plane associated with microstrip lines or strip lines. Avoid sharp right angle turns in microstrip
- Keep high speed circuits together and low speed circuits together. Keep I/O near the edge of the board where it will be used.
- Decoupling capacitors should be placed as near to the EMI source (chip) as possible. It will often be necessary to use two different capacitors since most high value capacitors have a physical structure that contains significant inductance. The capacitor should be evaluated as part of a series LC circuit containing the capacitance and the inductance of the capacitor leads and etch runs to the EMI source. The resonant frequency can be in the 10 MHz range for many typical capacitors. The designer must determine this resonance, and insure the resonant frequency is much higher than the frequency contained in the source to be decoupled.
- Use ferrite beads in the design to increase the impedance of power runs, at high frequencies. These are especially useful at frequencies where the capacitors are in resonance and no longer effective.

- All controlled impedance signal lines should be terminated in the proper impedance. Unterminated lines can cause standing waves at resonant frequencies which are good radiators.

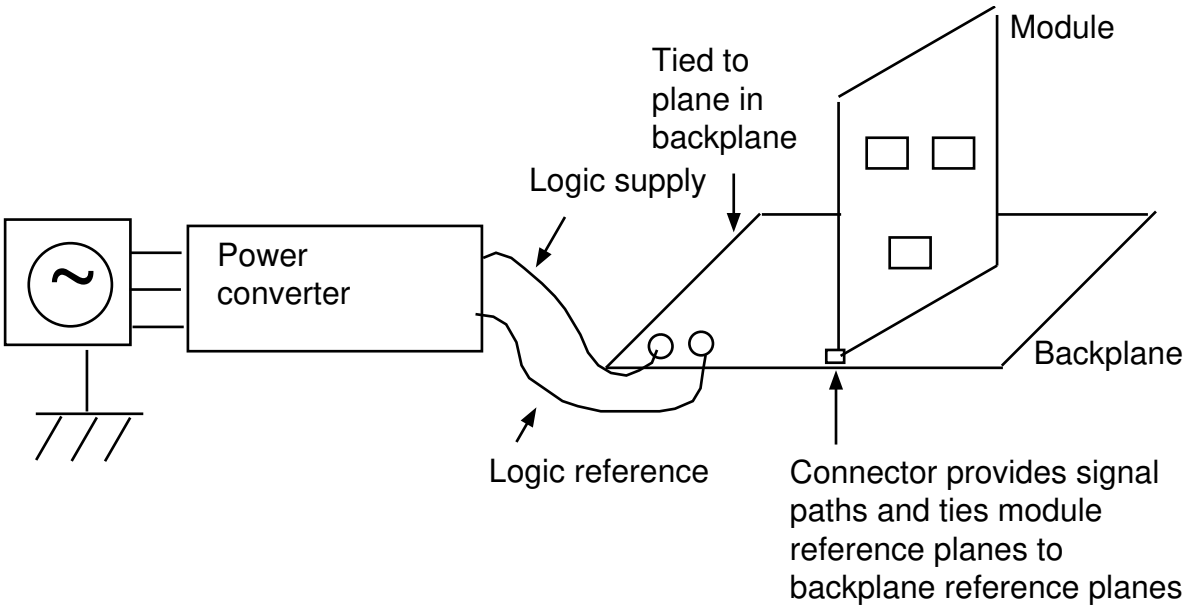
- Always use a chip package with reference planes between the chip and the heat sink. NEVER electrically couple the heat sink to the chip die. Use nonconductive heat sinks if possible.

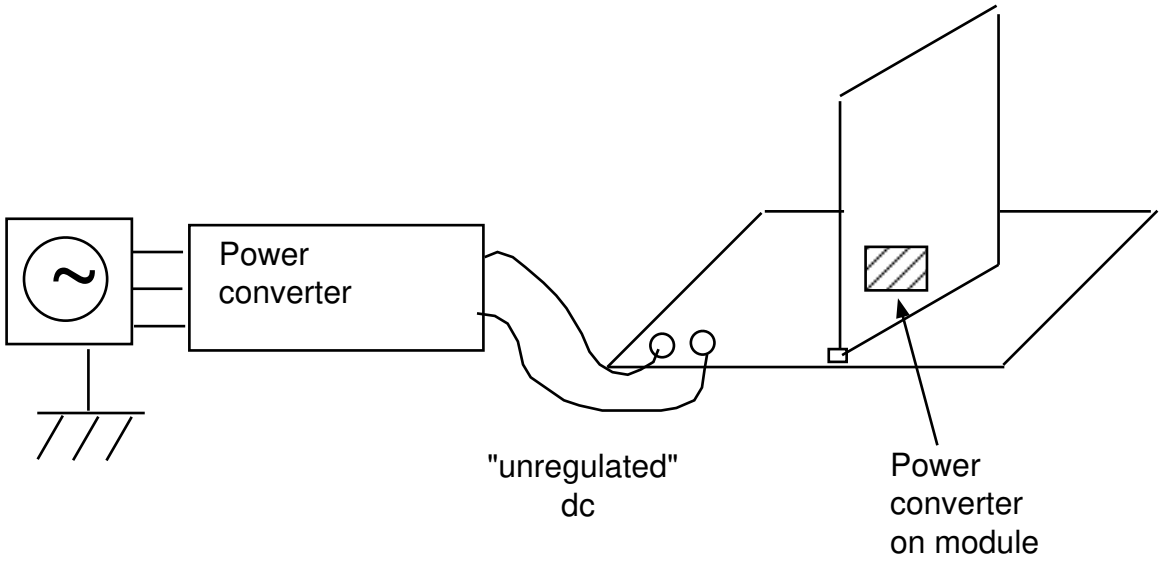
- Always insure a low impedance connection between the module reference plane and the shield of the enclosure closest to the I/O transceivers.

- Unbalanced I/O drivers should have their reference connected to the shield of the enclosure through a low impedance path and close to the I/O bulkhead.

11.3.3 Power Distribution Guidelines

Figure 11-9: Power Distribution Configuration





1. System
   The problems encountered in dc power distribution are similar to those encountered in the transmission of signals, except that power is usually more widely distributed.

   a. DC return leads should follow the dc power leads, in order to minimize the size of the loop formed.

   b. DC power leads should be separated from the primary (ac) power.

   c. DC power leads should be separated from the signal distribution paths.

   d. Logic reference should be isolated from earth.

   e. Laminated bus bars can provide a good low impedance connection between supply and load.

   f. Local regulation, that is, distributing a higher dc voltage (48 volts in Laser, for example) and providing dc-dc conversion and regulation on each module reduces the resistive loss in the distribution system. It improves local power quality by reducing the distance between the load and the regulator. It also adds complexity to the modules, and may provide an opportunity for supply offsets between modules.

   g. Ferrites may be used to increase the impedance of (long) power paths at high frequencies, thereby reducing the potential for EMI radiation.

2. Backplane

   a. Provide contiguous, uninterrupted logic reference planes to reduce the possibility of developing voltage across the logic returns.

   b. Provide a common localized connection between backplane logic reference, power supply logic reference, and enclosure I/O bulkhead.

   c. *Bulk* capacitance, such as *0.1* μ*F* and larger capacitors, are often placed on a backplane to help compensate for the inductance in the path between the supply and the backplane. **Note:** All discrete capacitors have intrinsic inductance and resistance which limit their effectiveness.

3. PWB

   a. Connection between PWB and backplane should be made with multiple contacts, uniformly distributed along the PWB edge, to provide a low impedance, distributed, connection.

   b. Contacts (pins) should be located in power/return pairs to minimize the differential impedance of the power path.

   c. Provide enough contacts for adequate current capacity. Pins are generally rated at 1

amp or less maximum current per pin. Refer to Chapter 5, *Connectors,* for more information.

d. Avoid splitting or breaking power or return planes. If done, there should be close ac coupling between the two sections. Any device that uses the voltages on both sides of the split should straddle the split.

e. Locating power and reference planes adjacent (and close) within PWB can increase the capacitance between them enough to improve the power distribution characteristics. Unfortunately, this can make it impossible to put signal layers between the planes, which improves the quality of the signal paths and virtually eliminates radiation (EMI) from the signals.

f. Locate fast chips near the regulator or the connector, where the power will be most stable.

g. High-frequency decoupling capacitors should be located near the ICs they are serving. Minimize dispersion etch between the cap's surface mount pads and the vias that go to the reference plane.

h. When multiple capacitors are needed for a chip, arrange them symmetrically around the chip.

i. The total capacitance value needed for an IC is commonly estimated by

$$C_{total} = \frac{i_{transient} \times \Delta T}{\Delta V}$$

$i_{transient}$ is the total transient current the IC draws during a switching event.

Δ T is the time interval that the decoupling caps must supply charge, approximately five times the IC signal risetime.

ΔV is the allowable droop of the supply voltage on the PWB.

In general,

-- at least one *0.1* μF per IC with 10 outputs or less

-- at least one *0.1* μF per 4 square inches of PWB

Low-frequency decoupling should also be on the PWB, but determining how much is more complicated. For example, NVAX/Calypso uses 1500 μF of low-frequency decoupling capacitance on the module.

j. See Chapter 4, *Non-IC Components,* for recommended capacitors.

Note that all capacitors have significant inductance, and so have a natural resonant frequency. A capacitor will not be effective at frequencies near or above its natural resonance. Leads, etch, or vias in the path between the capacitor and reference add inductance.

4. Package

   a. Locate leads or pins in power/return pairs, distributed around the package.

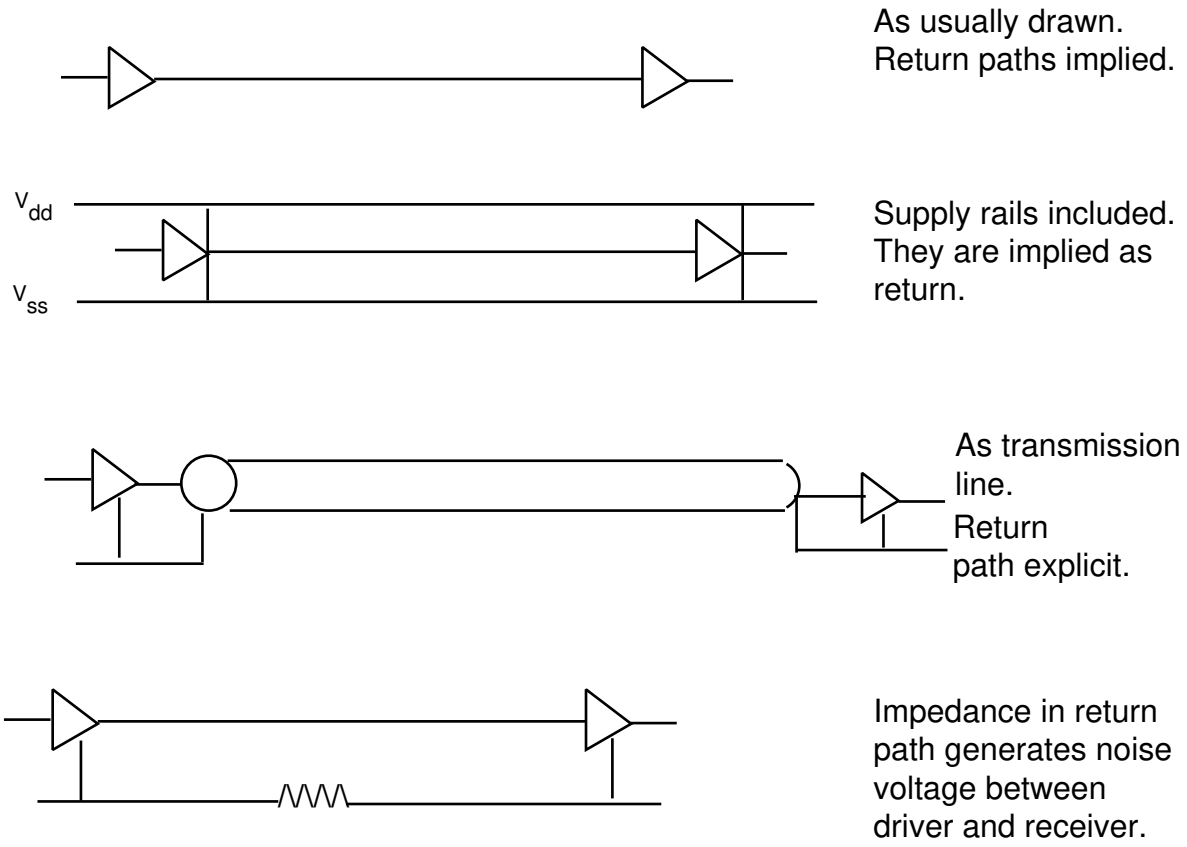
   b. In general, signal paths are less affected by lead or pin length than V_{dd} and V_{ss} and will be, so the shorter leads or pins should be used for power distribution.

   c. ICs in packages with shorter power and return pins will generally have reduced simultaneous switching noise problems. For instance, a square package is generally better than a dip, and a dip with center power/return pins is better than one with "standard" corner power/return pins.

   d. On-chip decoupling is much more effective than package mounted decoupling caps. See *On-chip Capacitance vs. Package Capacitors, Design Tradeoffs for Reducing Simultaneous Switching Noise in CMOS*, by Judy Chen, for discussion and recommendations for decoupling.

11.3.4 Signal Return Path Guidelines

Figure 11-10: Closed Loops for Signal Transmission



Transmitting a signal requires a closed loop between driver and receiver. The quality of the return side of the loop is no less important than that of the signal side.

- Some portion of the power network usually provides the signal return path.
- In most cases, V_{dd} and V_{ss} are equivalent at high frequency, (that is, for the signal return) because of the relatively tight coupling between them.
- In a PWB, the signal return current will usually travel in the nearest plane, underneath the signal line's path. Planes provide the best return path in PWBs.
- Avoid any discontinuities in the return path. For instance, do not run signal lines over splits or breaks in a (adjacent) plane, unless the high-frequency coupling across the split is good.
- Avoid introducing discontinuities when going through connectors of any sort. The loop formed by the signal and its return should be kept small. For instance in a connector, the reference pins should be close to their related signal pins.

- Best signal transmission quality is obtained when the return path is explicitly provided, as it is in coaxial cables and twisted pairs, for example.

- In Figure 11-10, note that the return path is always connected at both ends, even though this may cause a *ground loop,* it is a closely coupled loop. A loop is a problem only when the loop area is large, as is likely in an ill defined return path.

- Good return paths are just as important for controlling EMI as for controlling signal quality.

Differential signaling extends the signal/return idea by running two coupled signal paths between the driver and receiver, and driving the signal on one and its complement on the other. The receiver detects the difference between the two to determine the logic state. In single-end signaling, the receiver compares the input signal to a reference voltage (derived from V_{dd} and V_{ss}) to determine logic state, and thus is susceptible to any noise on those reference voltages, and to any offset between the reference voltage used at the driver and the reference at the receiver. Differential signaling thus provides the following advantages.

- Within the common-mode noise-rejection capability of the receiver, the need for a stable common reference voltage between driver and receiver is removed. This is advantageous for longer distances or communication between components that might have different power supplies or reference voltages.

- The power source transient currents generated in the driver are reduced, because a signal and its complement are always being driven.

Differential signaling requires two complete paths for each signal to be transmitted.

11.3.5 Reflection from an Impedance Mismatch

Figure 11-11: Reflection from an Impedance Mismatch

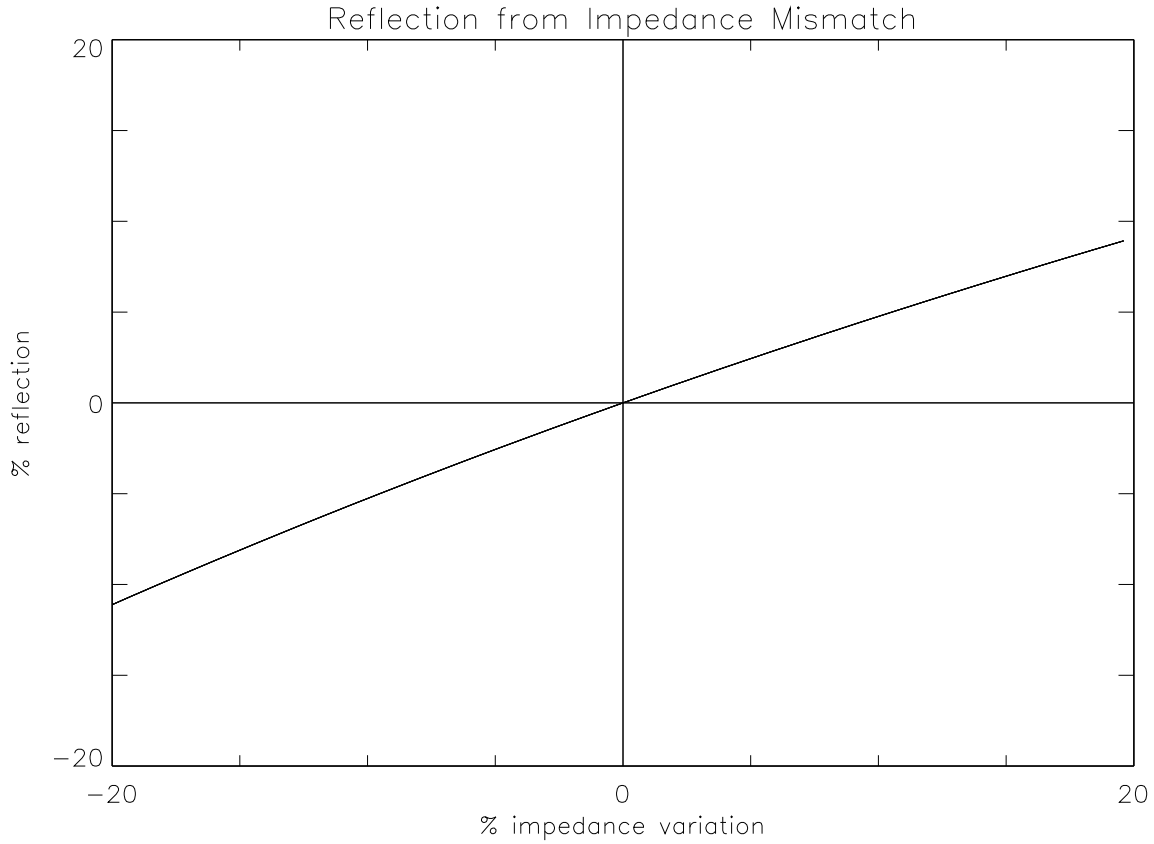


Figure 11-11 shows the relative voltage reflected from a sudden change in transmission line impedance,

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

11.3.6 Safe Limits for Total Line Length and Loading

If the total propagation delay through a network is small enough, all transmission line effects can be safely neglected. “Small enough” is defined relative to the rise and fall times of the signals that are to be carried.

When these limits are exceeded, the signal path behaves as a transmission line, and further analysis will be required. The lengths in the following figures are calculated by

$$l_{max} = \frac{-C_{load} + \sqrt{C_{load}^2 + 4C_0 t / L_0}}{2C_0}$$

C_0 and L_0 are the capacitance and inductance of the line per inch
C_{load} is the added load capacitance (that is, logic device inputs) per inch
t is the appropriate fraction of the signal risetime

See *the Electrical Design Guide for Printed Circuits* for more extensive length limits for TTL networks.

For data, address, control, and bus signals it may be safely required that the total delay be less that $t_r/2$. Similarly, for asynchronous control signals the required delay is less than $t_r/5$, and for clocks, the required total delay is less than $t_r/10$. These limits are plotted in the following figures for risetimes of 0.5, 0.75, 1.0 and 2.0 ns.

Figure 11-12: For Data, Address and Control Signals, Total Delay Less Than $t_r/2$

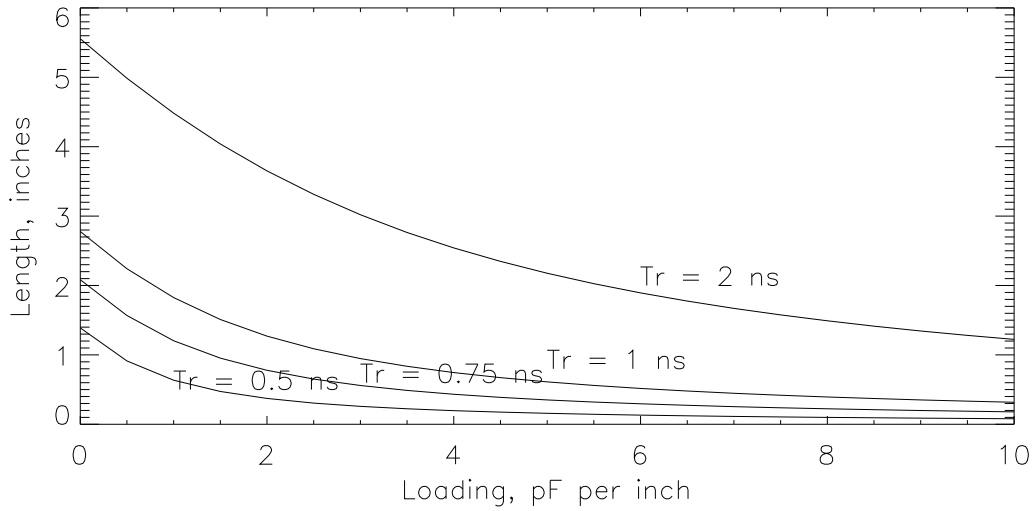


Figure 11-13: For Asynchronous Control Signals, Total Delay Less Than t_r/5

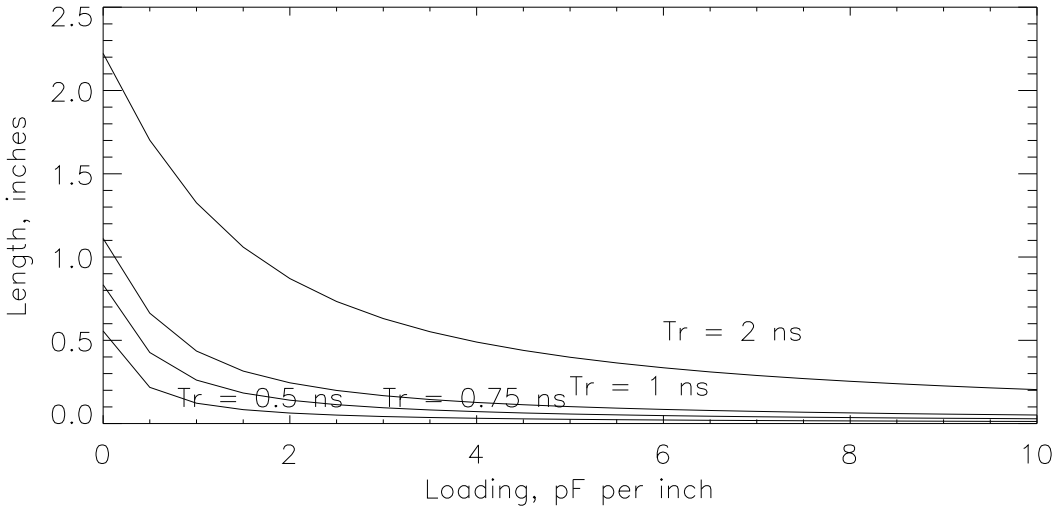
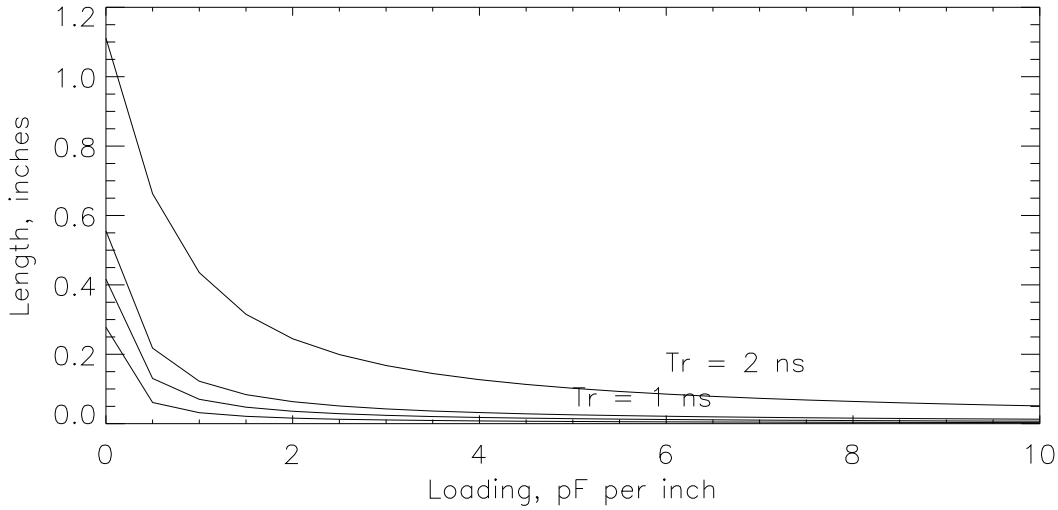


Figure 11-14: For Clock Signals, Total Delay Less Than t_r/10



11.3.7 Safe Coupled Line Length

The amplitude and duration of crosstalk signals depend strongly on the length over which the transmission lines are coupled. If the length is small enough, crosstalk effects can be neglected.

Limits on coupled length may be calculated using the receiving device's dc thresholds. For example, considering only near-end crosstalk from one line to another,

$$l_c(max) = \frac{V_{threshold} t_r}{2 K_b t_p V_i}$$

if the crosstalk voltage exceeds the device threshold $(K_b V_i > V_{threshold})$

Refer to Chapter 6, *Printed-Wiring Boards*, for illustrations of microstrip and stripline construction, and for values for crosstalk coefficients. This can be extended to cases of unterminated and series terminated lines with two or four active neighboring lines, at varying spacings. Tables 11-3 and 11-4 show example calculated maximum coupled line lengths for microstrip lines for some of these cases. *No limit* indicates that the crosstalk pulses do not cross the receiver threshold.

Table 11-3: DC Threshold Limits for Microstrip

Driver risetime = 2ns, voltage swing = 3.0v threshold = 0.5v				
Line Width	**Dielectric thickness**	**Line Space**	**2 Neighbors**	**4 Neighbors**
Unterminated Lines				
5 mils	8 mils	5 mils	4.6 inches	3.6 inches
		10	8.7	7.0
		15	no limit	11.8
		20	no limit	no limit
Series Terminated Lines				
5 mils	8 mils	5 mils	9.1 inches	7.2 inches
		10	no limit	no limit
		15	no limit	no limit
		20	no limit	no limit

Table 11-4: DC Threshold Limits for Stripline

Driver risetime = 2ns, voltage swing = 3.0v threshold = 0.5v				
Line Width	**Dielectric Thickness**	**Line Space**	**2 Neighbors**	**4 Neighbors**
Unterminated lines				
5 mils	8 mils	5 mils	3.2 inches	2.6 inches
		10	4.8	4.1
		15	7.2	6.5
		20	10.8	10.2
Series Terminated Lines				
5 mils	8 mils	5 mils	6.4 inches	5.1 inches
		10	9.6	8.3
		15	no limit	no limit
		20	no limit	no limit

If the response time of the receiving device is considered, the dc threshold is not an absolute limit. A pulse of sufficiently short duration can cross threshold without causing the receiver to switch. This is called the ac noise immunity (ACNI), and has units of (volts x time).

Calculated using the ac noise immunity (and still considering the dc thresholds), the example length limits when $l_c > t_r/2t_p$ are

$$l_c(max) = \frac{ACNI}{(K_b V_i - V_{threshold})2t_p}$$

and when lc < tr/2tp,

$$l_c(max) = t_r \left[\frac{V_{threshold} + \sqrt{V_{threshold}^2 + 4K_b V_{ir} ACNI}}{K_b V_i 4t_p} \right]$$

These lengths are shown in the following tables.

Table 11-5: AC Noise Immunity Limits for Microstrip

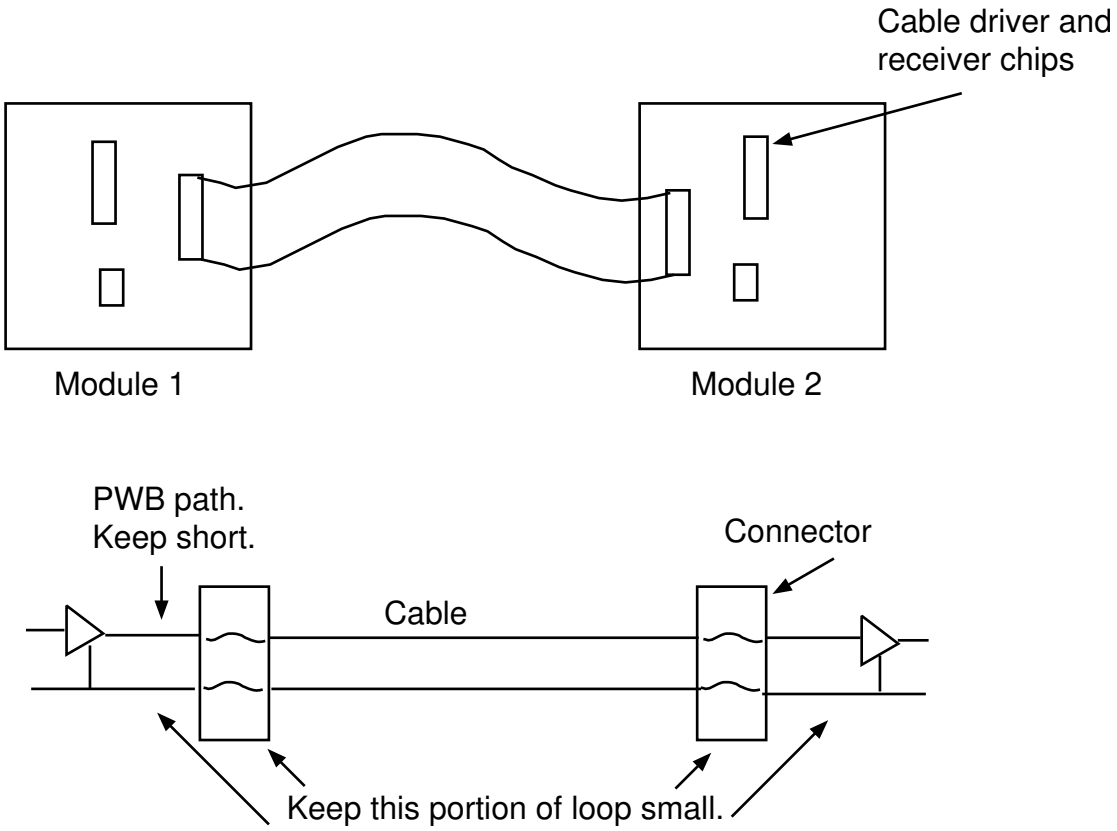
Driver risetime = 2 ns voltage swing = 3.0v Noise immunity = 2.0 v-ns, threshold = 0.5v				
Line Width	**Dielectric Thickness**	**Line Space**	**2 Neighbors**	**4 Neighbors**
Unterminated Lines				
5 mils	8 mils	5 mils	6.8 inches	5.9 inches
		10	10.1	8.8
		15	no limit	12.3
		20	no limit	no limit
Series Terminated Lines				
5 mils	8 mils	5 mils	10.4 inches	9.0 inches
		10	no limit	no limit
		15	no limit	no limit
		20	no limit	no limit

Table 11-6: AC Noise Immunity Limits for Stripline

Driver risetime = 2 ns voltage swing = 3.0v Noise immunity = 2.0 v-ns, threshold = 0.5v				
Line Width	**Dielectric Thickness**	**Line Space**	**2 Neighbors**	**4 Neighbors**
Unterminated LInes				
5 mils	8 mils	5 mils	5.2 inch	4.5 inch
		10	6.6	6.0
		15	8.9	7.9
		20	10.5	10.6
Series Terminated Lines				
5 mils	8 mils	5 mils	7.9 inch	6.8 inch
		10	10.2	9.3
		15	no limit	no limit
		20	no limit	no limit

11.3.8 Cable/Connector Recommended Configuration

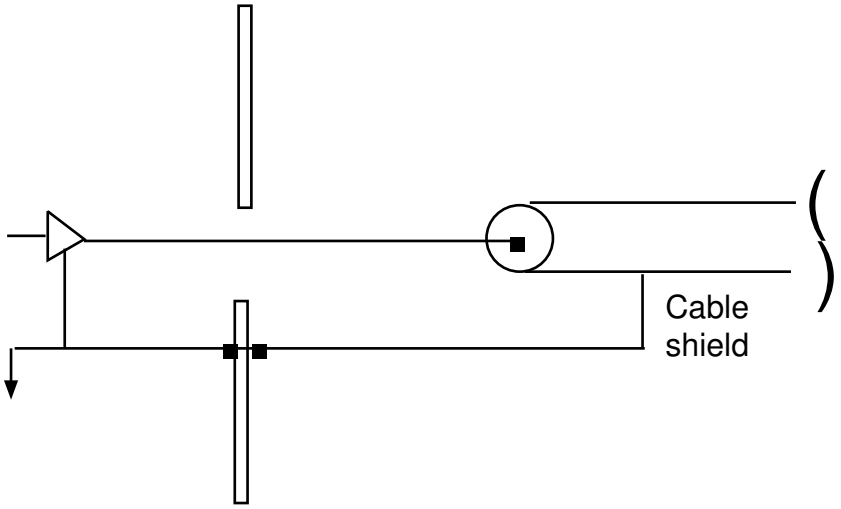
Figure 11-15: Cable/Connector Recommended Configuration



- Logic reference lines in the cable must be connected as directly as possible to the driver and receiver for the associated signal line. There should ideally be as many returns provided as signal wires, and they should be evenly distributed through the cable and connector.
- The logic reference (return) lines in the cable should be connected at both ends,. It is important to maintain a well defined, closely coupled return path.
- The logic references of all the driver/receiver components for a particular cable must be interconnected to ensure that no dynamic potential differences can be developed. For instance, they should share the same power and reference planes on the PWB. It is important to ensure tight coupling between the interfacing component's logic reference and that of the signal cable.

- ICs that drive or receive the cable should be close to the connection to the cable, such that length x t_{pd} < tr/4.
- Transmission line losses will become significant when cables get long. The maximum possible data rate for a cable of given length can be limited by the conductor (skin effect) losses. Increasing the size of the conductors can compensate for this.
- Keep signals with different functions and different time dependencies away from each other within the cable. Keep clocks away from asynchronous control, away from data, address, and control, and so forth.
- The signal to reference ratio within the cable can have a significant effect on the signal quality.

Figure 11-16: I/O Recommended Configuration



- It is desirable to provide a single, common entry and exit point for each enclosure for all cables that must cross the enclosure boundary, called the I/O interface bulkhead. This bulkhead should provide a common reference plane for any signal or power cable filtering or shielding. No other enclosure reference for cable shields or filters should be used.
- The shield of the cable should be connected to the I/O bulkhead at both ends of the inter-enclosure cable run. It may be necessary to provide a capacitively coupled reference connection at one end to avoid problems caused by connecting two different primary power references (creating the classic "ground loop") If unshielded cable is to be used, suitable filtering must be provided, both to stop noise from getting into the system and to control any EMI causing energy coming out.

- Logic devices that drive or receive the I/O signals should be referenced as directly as possible to the bulkhead. It is desirable to mount these parts directly on the bulkhead. (Note that these first recommendations can reduce or eliminate the need for additional filtering on the I/O signal lines.)

- DC coupling of signals is a problem if there are supply/reference voltage offsets between the devices that are connected. The offset will reduce the signal noise margin, and will cause potentially significant currents to flow in the cable's reference lines. ac coupling eliminates these problems but complicates the design.

- Differential signaling can be especially useful for I/O.

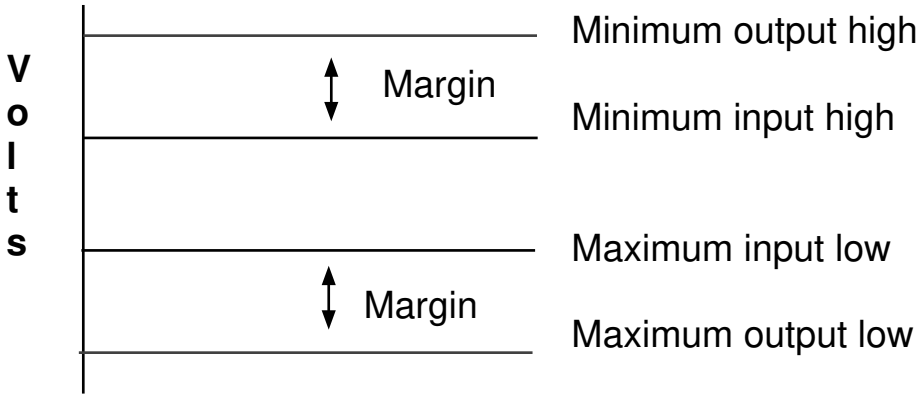
- Optical signaling eliminates all electrical shielding and isolation related problems.

11.4 Noise and its Effects

In order to do effective electrical design, it is important to remember that digital circuits are built using analog parts, and that the analog characteristics of those parts will become significant in determining both the amount of noise or distortion that is generated and how that noise or distortion will affect other circuits.

11.4.1 Analog Characteristics of Digital Logic

Figure 11-17: Thresholds and Noise Margins



DC thresholds are commonly specified for logic devices, defining the maximum input voltage that will be interpreted by the device as “low” and the minimum input voltage that will be interpreted as “high”. These thresholds are normally specified such that variations caused by the IC manufacturing process and reasonable variations in temperature and supply voltage are covered. ng process and reasonable variations in temperature and supply voltage are covered.

Noise margin is the difference between the specified worst-case output levels and the associated specified input levels. This is the guaranteed safety margin against noise. (See Figure 11-17.) Note that driver and receiver are not necessarily from the same IC family, and so the noise margin must be determined accordingly. Similarly, driver and receiver(s) may be operating on different supply voltages (for example, +5 volt RAMs on a 3.3 volt bus). These require special attention to input and output level, and the presence and reference voltage of clamping diodes.

The dc margin is reduced by the presence of noise, both dc and ac, on the signal and reference paths of the interconnect over which the ICs communicate.

Figure 11-18: Transfer Characteristic

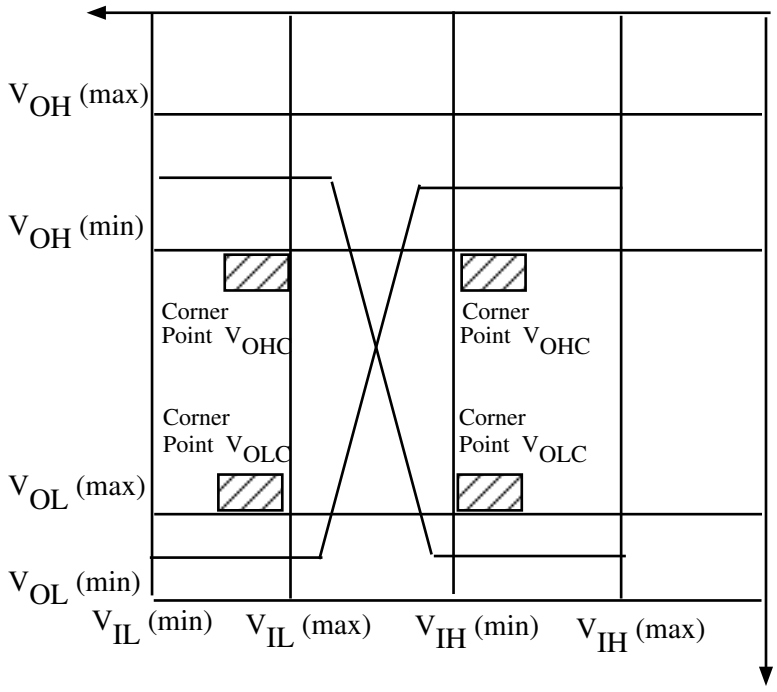


Figure 11-18 shows an example transfer characteristics for a typical logic gate. Note that there is a region where the output is a linear function of the input, that is, where the device acts as an amplifier. In general, this region can fall anywhere between the specified input thresholds of the device, and will have a width that depends on a number of factors. When the input is in this linear region, the device is very susceptible to noise and can in some cases become unstable and oscillate. It is desirable to set a limit on how long an input can stay in this region.

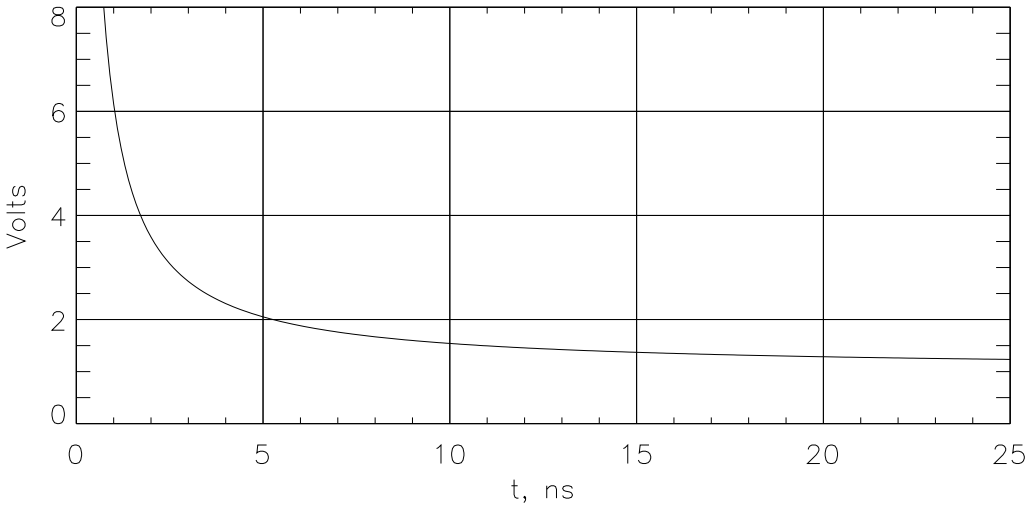
The non-zero response time of logic devices means that the dc thresholds are not absolute limits. A pulse of sufficiently short duration can cross a threshold without causing the gate to switch. This is called the ac noise immunity. Figure 11-19 shows the measured ac noise immunity of a TTL inverter. Plotted is the pulse amplitude and duration combinations that cause the gate to respond. Pulses of smaller amplitude or duration cause no response.

Table 11-7 lists some of the useful electrical performance parameters for commonly used IC families. These are representative values, specific portions of specific IC's may vary considerably

Table 11-7: Characteristics of I/O Drivers and Receivers

IC family	Risetime (Min)	R_s(low) Ω	R_s(high) Ω	C_{in} pf	$C_{I/O}$ pf	Safe input V	input clamp
FTTL	2 ns	7	200			-0.5, + 7v	
ACT	2	20	20	4.5	16	-.5, +7	20 mA max
BCT	1	7	130		7 - 12	-.5, +7	20 mA max
FCT	1	5	130	6 - 10	8 - 12	-.5, +7	20 mA max
ABT	1	8	90	4	8	-.5, +7	20 mA max

Figure 11-19: Measured AC Noise Immunity of 74S00



11.4.2 Noise Timing

Not all inputs are sensitive to noise at all times. Edge sensitive inputs, such as clocks, latches, and other similar signals, must be protected from noise at all times. Inputs that are clocked or latched are only vulnerable during the clock or latch setup and hold times. Noise at other times is of little concern. Thus, the timing of noise relative to system operation is important, and assuming that noise margin must be maintained on all signals at all times is unnecessarily restrictive.

It is also necessary to consider whether the noise generated by different sources will add together. Assuming that all noise contributors add at all times is also unnecessarily restrictive. Taking a simple viewpoint, crosstalk and simultaneous switching noise might add because they are both directly caused by IC switching activity. Reflections and other transmission-line distortions would not add to these because the timing of the reflections is controlled by the length and configuration of the lines.

11.5 Signal Characteristics

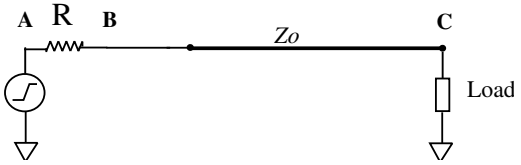
The following sections contain waveform examples for useful combinations of network configuration and termination.

11.5.1 Assumptions

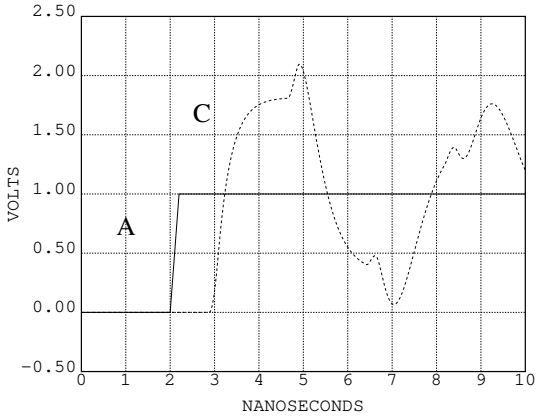
- The source impedance of the drivers is $R_{dr} = 5\ \Omega$;
- The receiver (load) input impedance is $R_L \parallel C_L$ where $R_L = 50\ k\Omega$ and $C_L = 6\ pF$. These values are typical for CMOS;
- The signal risetimes are selected to be 2 ps and 0.2 ps. The latter is quite a short one, but it is used for illustration purposes;
- The input signal "ON" state is normalized to +1 V, and the "OFF" state is 0 V;
- Most transmission lines are selected to be 5 inches long, with propagation delay of 0.884 ns. Other lengths will be explicitly specified in the text. The characteristic impedance is $Z_o = 50\ \Omega$.

11.5.2 Point-To-Point Topology

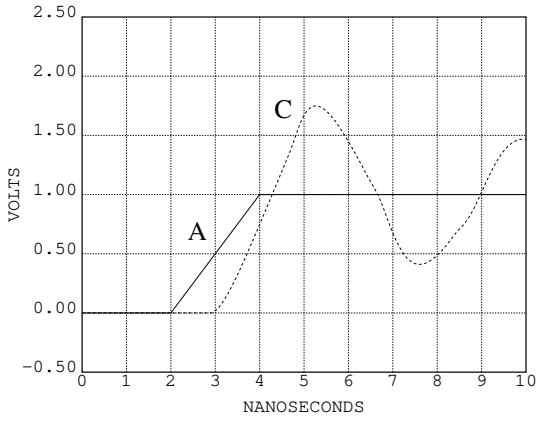
Unterminated



Almost open-circuit conditions. Strong reflections on both ends of the transmission

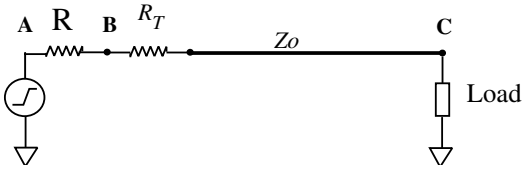


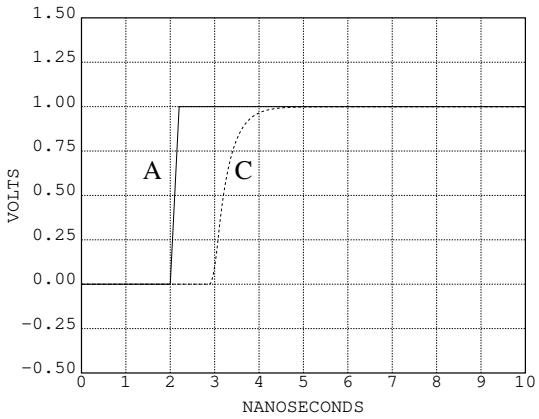
Unterminated, risetime = 0.2 ns



Unterminated, risetime = 2 ns

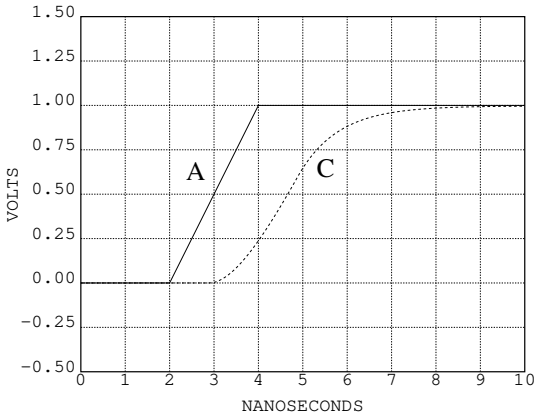
Series Termination





No overshoot

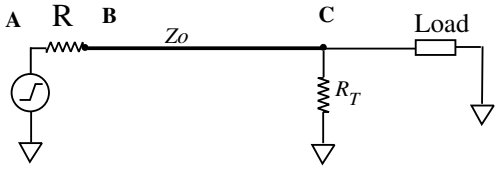
Series termination, risetime = 0. 2 ns



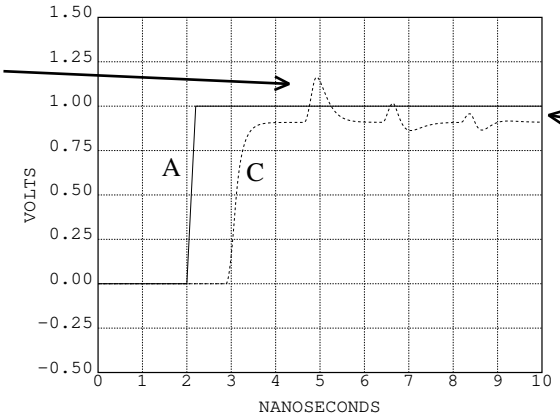
No overshoot

Series termination, risetime = 2 ns

Parallel DC Termination

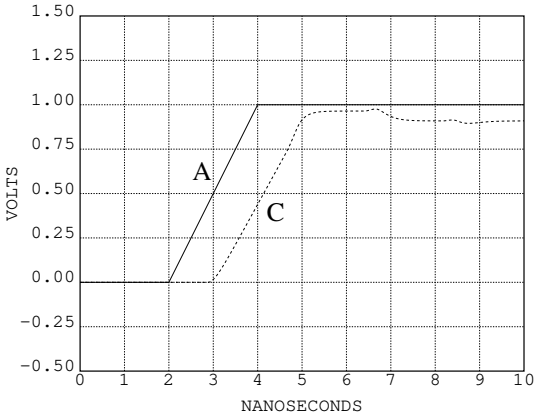


Note reflections caused by load capacitance and mismatch between R_S and Z_O.



Note dc level shift

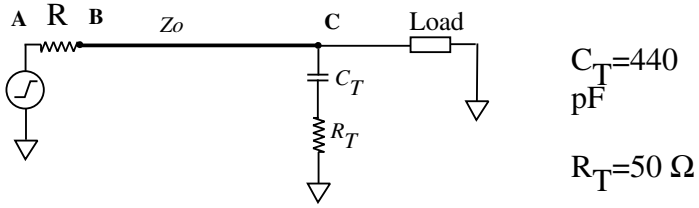
Parallel dc termination, risetime = 0.2 ns



Note dc level shift

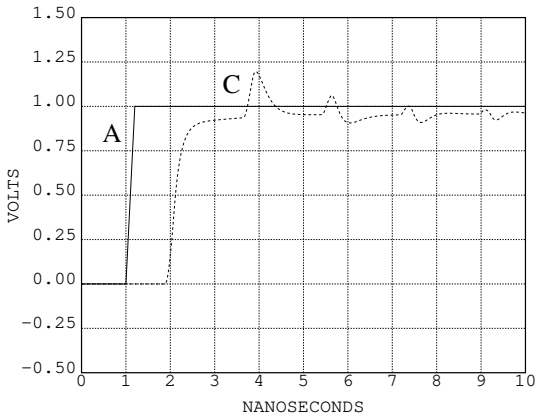
Parallel dc termination, risetime = 2 ns

Parallel AC Termination

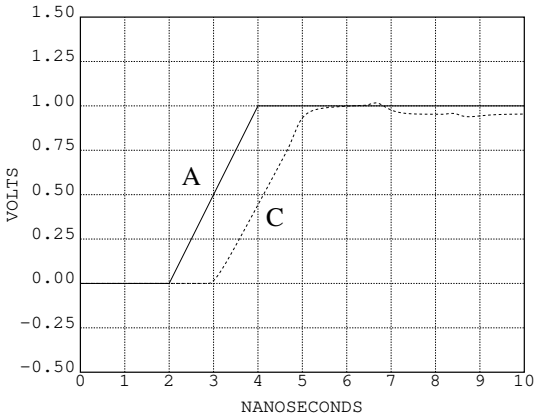


C_T=440 pF

R_T=50 Ω

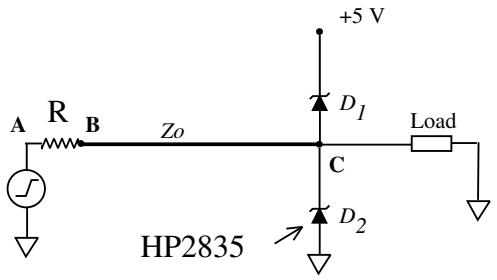


Parallel ac termination, risetime = 0.2 ns

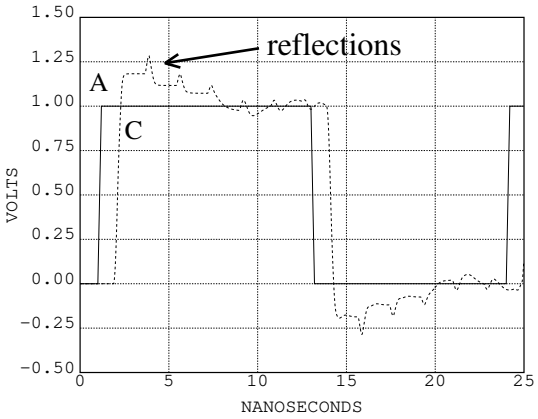


Parallel ac termination, risetime = 2 ns

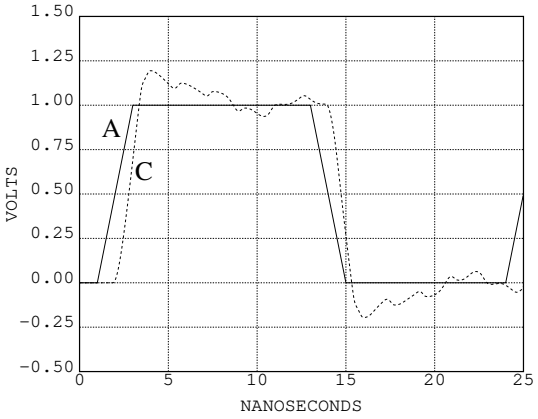
Parallel Diode Termination



Note overshoot caused by diode's characteristics.



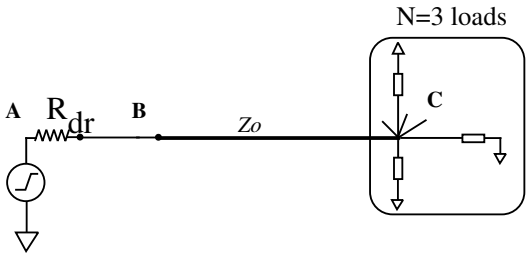
Parallel diode termination, risetime = 0. 2 ns

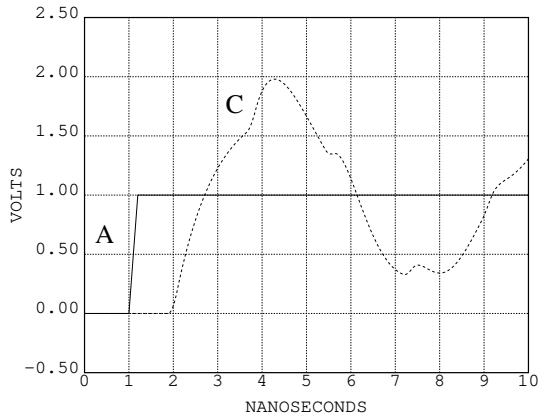


Parallel diode termination, risetime = 2 ns

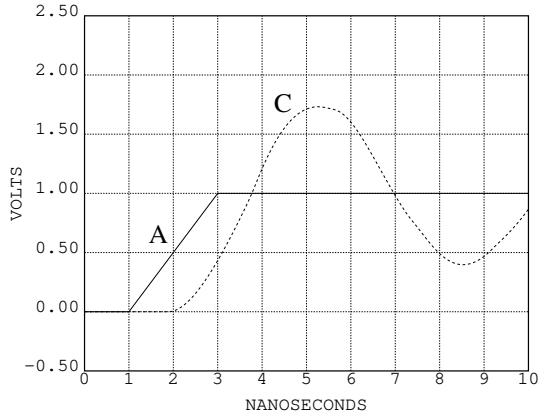
11.5.3 Point-To-"Lumped" Topology

Unterminated



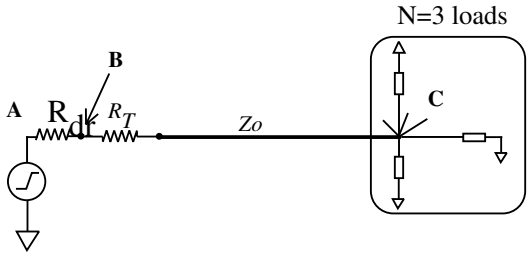


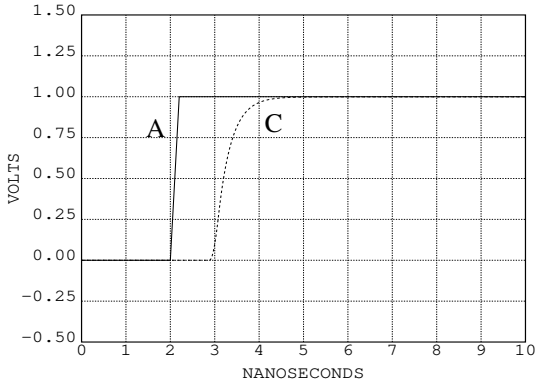
Unterminated, risetime = 0.2 ns



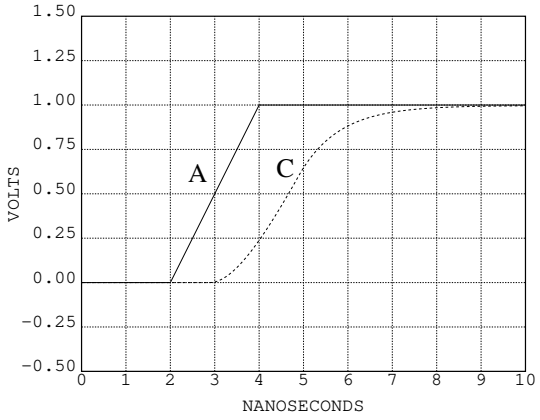
Unterminated, risetime = 2 ns

Series Termination



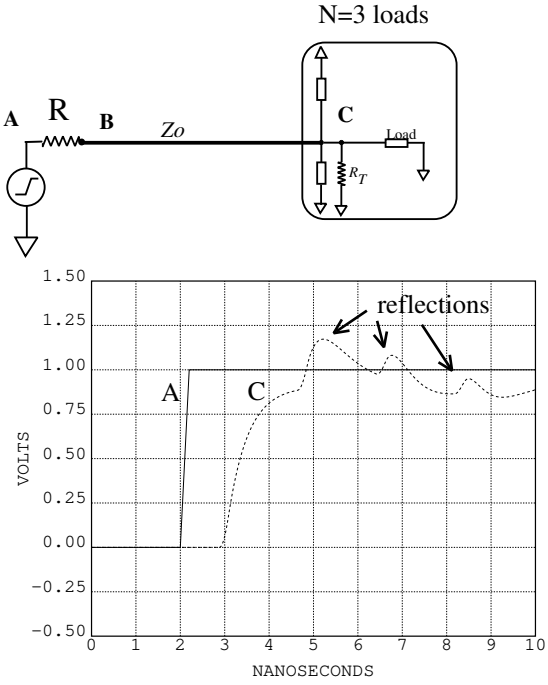


Series termination, risetime = 0.2 ns

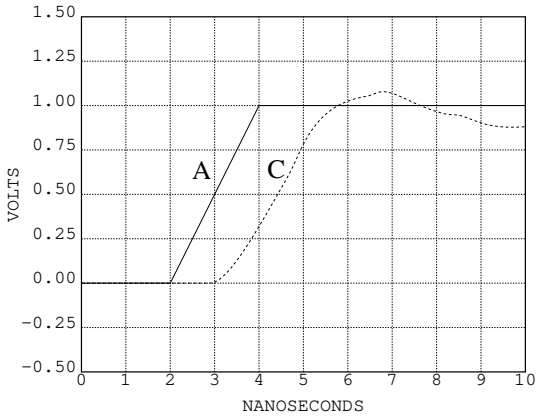


Series termination, risetime= 2 ns

Parallel dc Termination

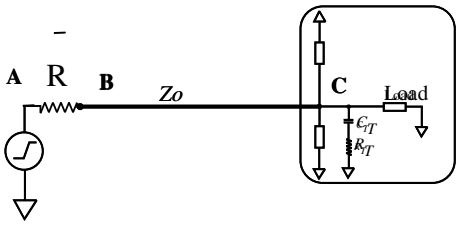


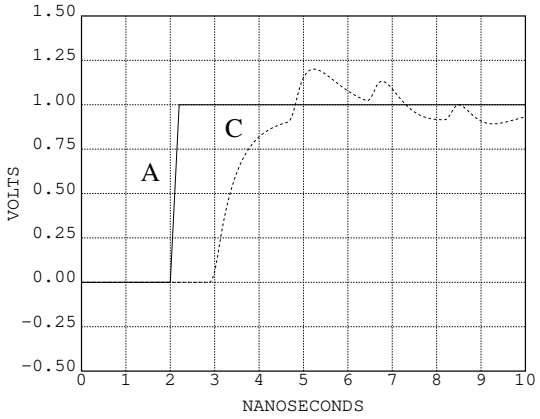
Parallel dc termination, risetime = 0.2 ns



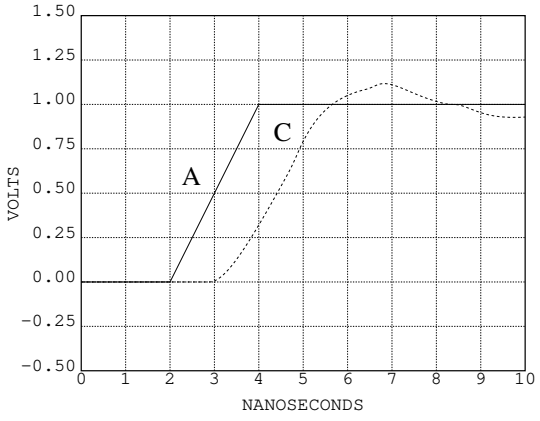
Parallel dc termination, risetime = 2 ns

Parallel AC Termination



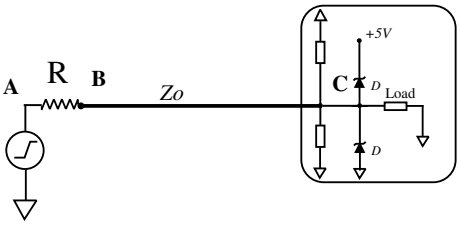


Parallel ac termination, risetime = 0.2 ns

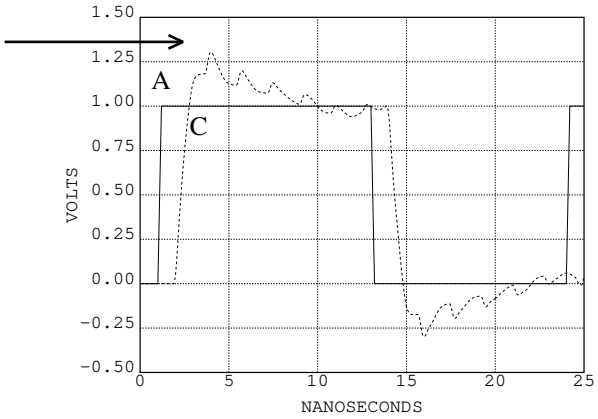


Parallel ac termination, risetime = 2 ns

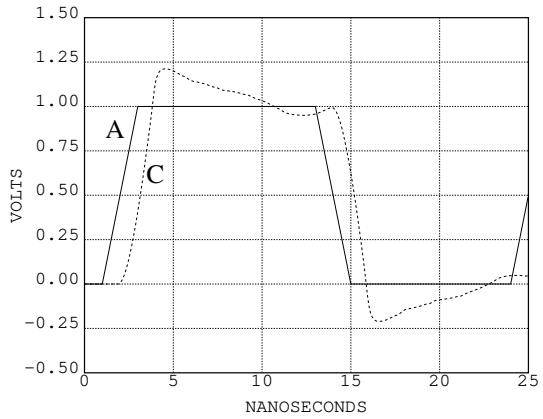
Parallel Diode Termination



Reflection from load and R_s -- Z_o mismatch.



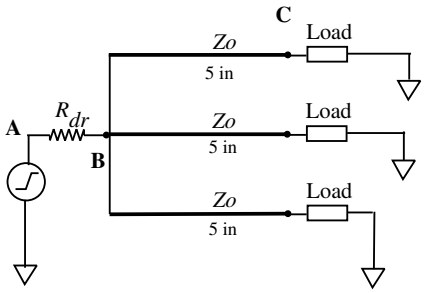
Parallel diode termination, risetime = 0.2 ns

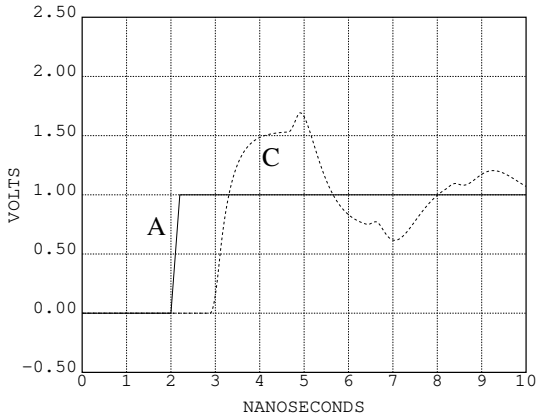


Parallel diode termination, risetime = 2 ns

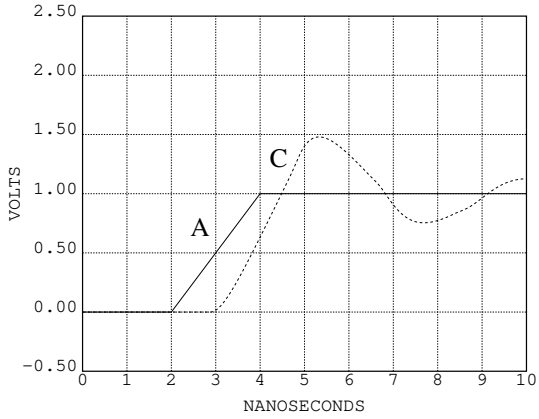
11.5.4 Star Topology

Unterminated



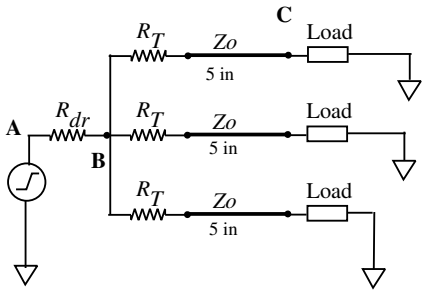


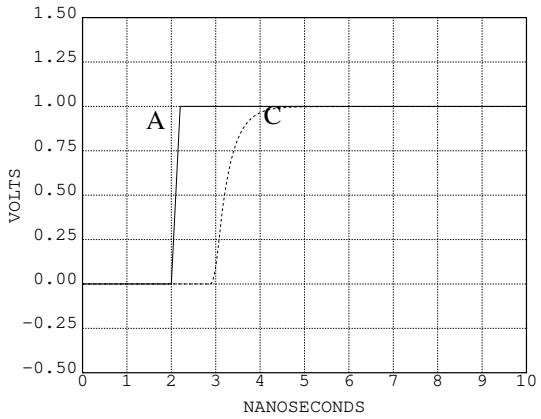
Unterminated, risetime = 0.2 ns



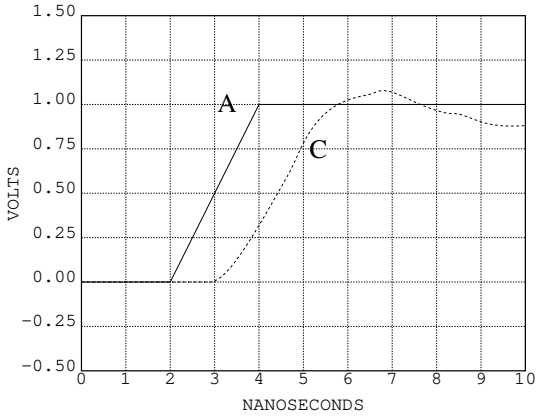
Unterminated, risetime = 2 ns

Series Termination



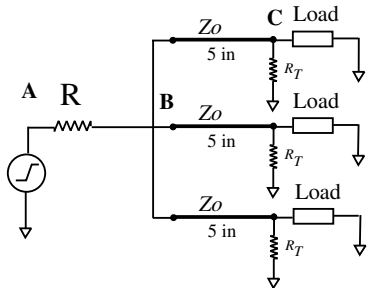


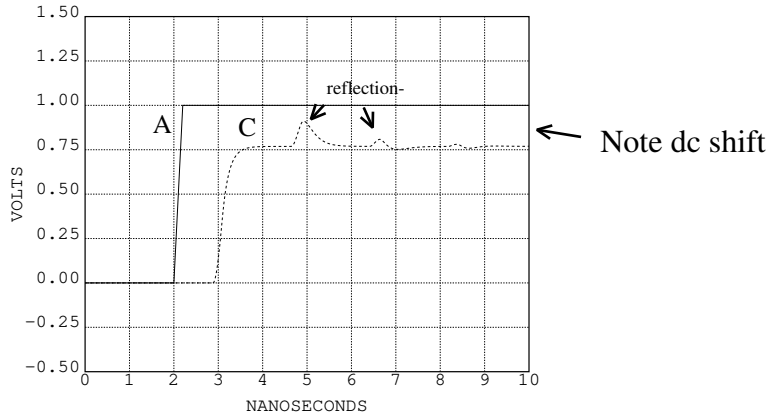
Series termination, risetime = 0.2 ns



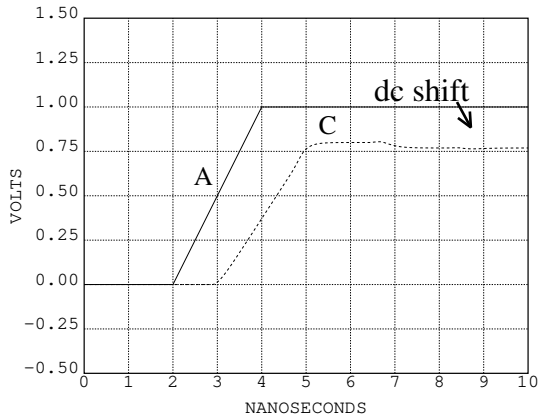
Series termination, risetime = 2 ns

Parallel dc Termination



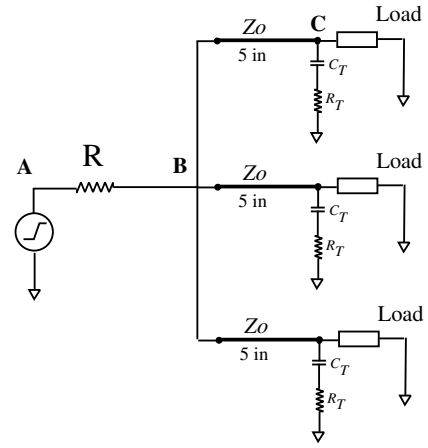


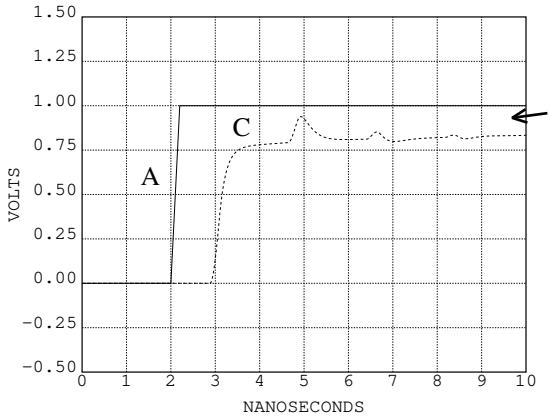
Parallel dc termination, risetime = 0.2 ns



Partallel dc termination, risetime = 2 ns

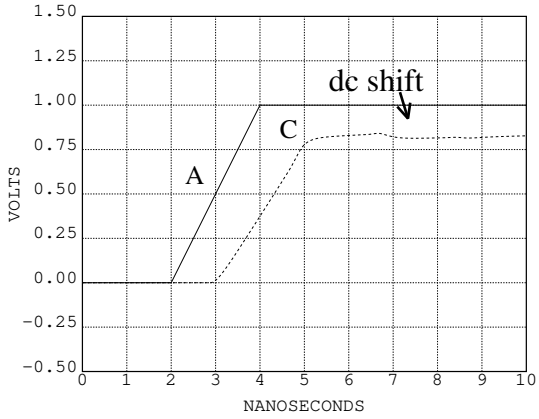
Parallel AC Termination





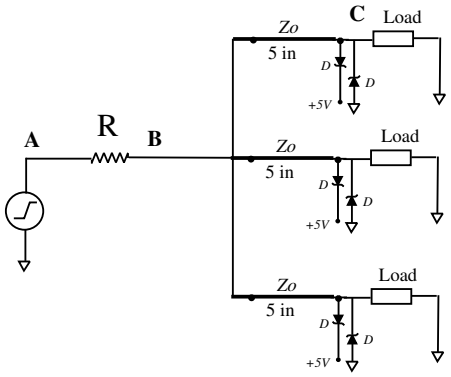
dc shift, slowly decreasing.

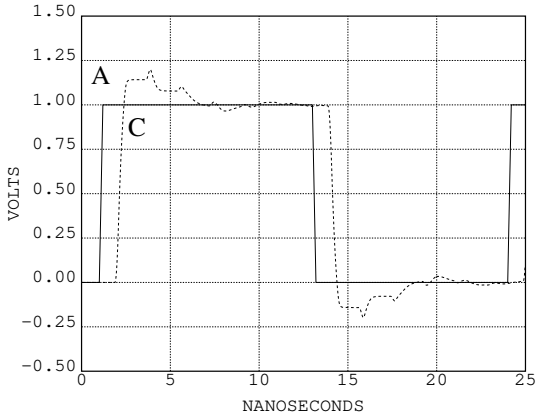
Parallel ac termination, risetime = 0.2 ns



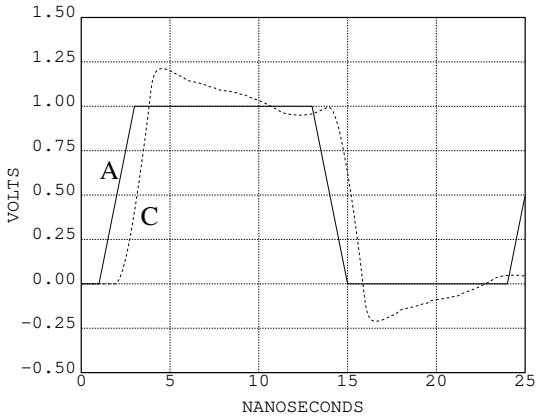
Parallel ac termination, risetime = 2 ns

Parallel Diode Termination





Parallel diode termination, risetime = 0.2 ns



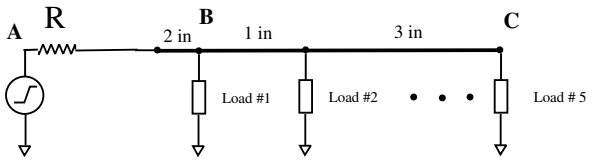
Parallel diode termination, risetime = 2 ns

11.5.5 Multiload Topology

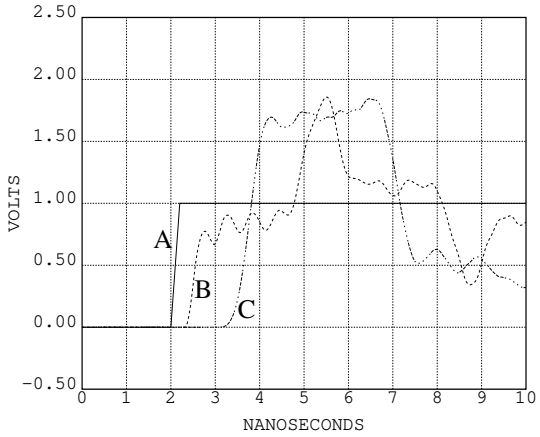
In this topology the loads are distributed along a transmission line, with the connecting stubs kept very short.

For the SPICE simulations the number of loads was chosen to be 5, with distances as indicated in the figure.

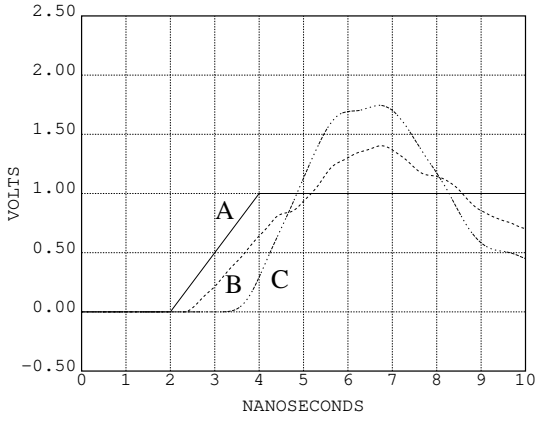
Unterminated



Multiple reflections, C doubles in voltage before B.

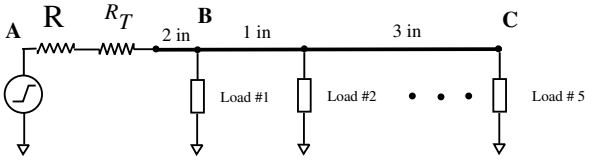


Unterminated, risetime = 0.2 ns

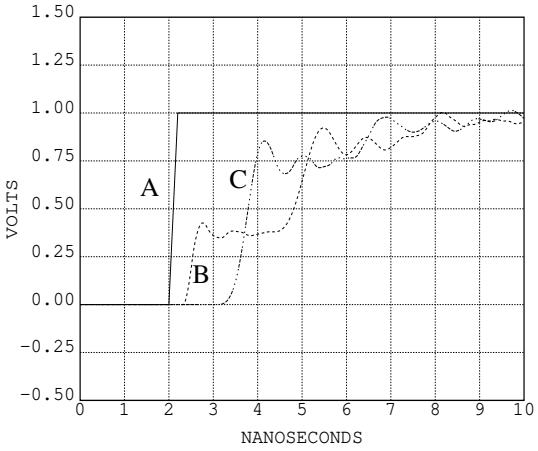


Unterminated, risetime = 2 ns

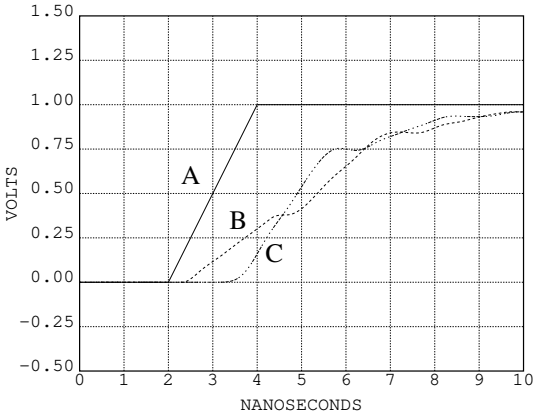
Series Termination



Note plateau at B caused by voltage division between R_s and Z_o. C will cross threshold before B.

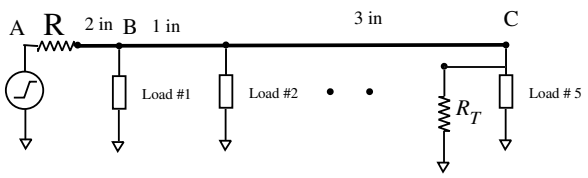


Series termination, risetime = 0.2 ns

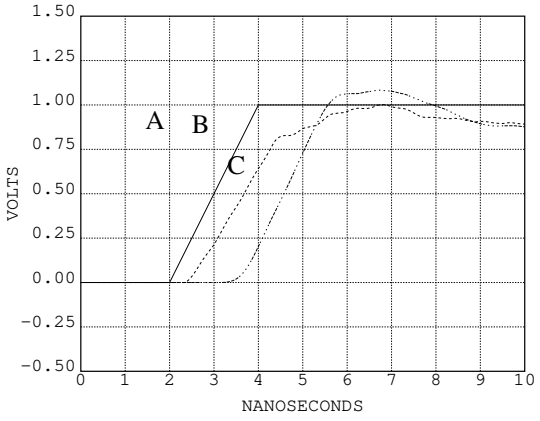


Series termination, risetime = 2 ns

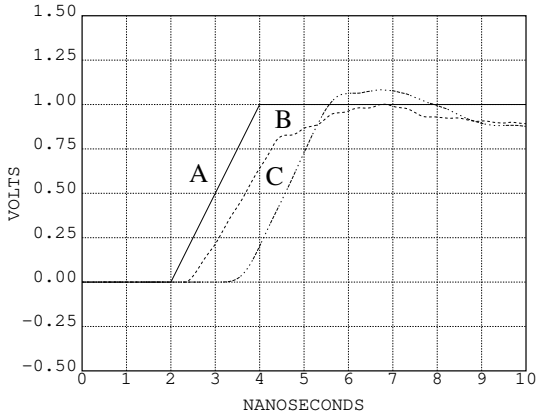
Parallel DC Termination



"Ringing" at B is caused by reflections between loads.



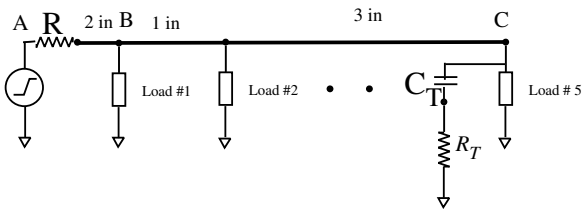
Parallel dc termination, risetime = 0.2 ns

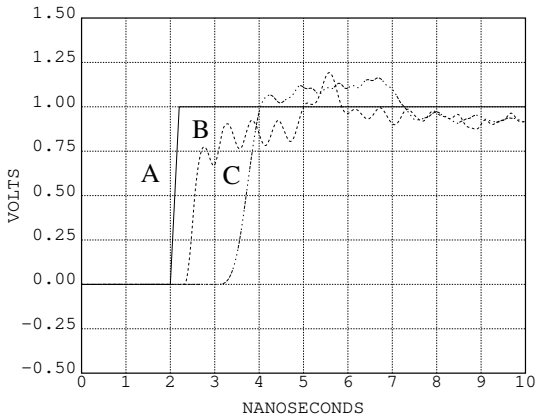


Parallel dc termination, risetime = 2 ns

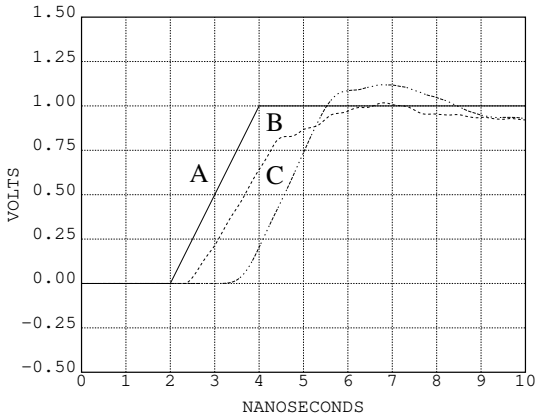
Note dc offset

Parallel AC Termination



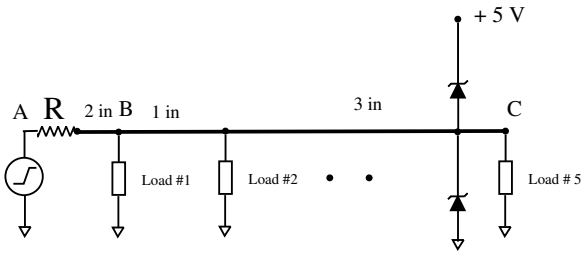


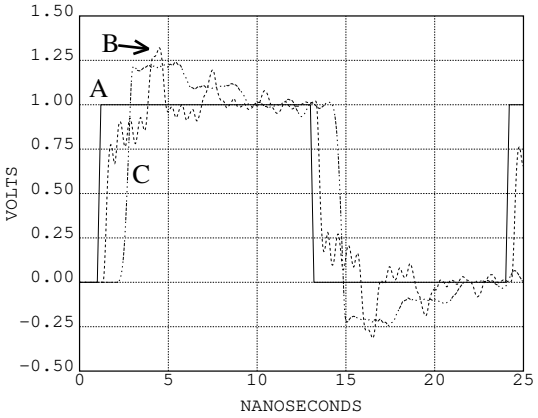
Parallel ac termination, risetime = 0.2 ns



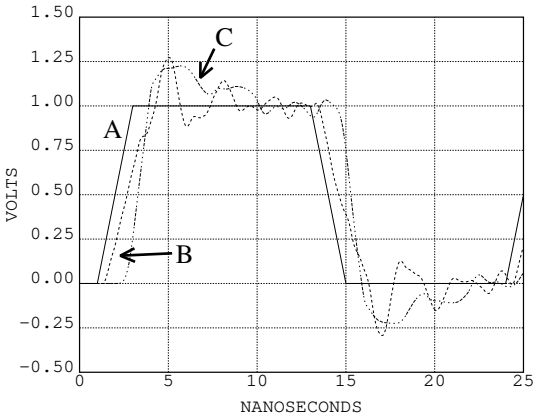
Parallel ac termination, risetime = 2 ns

Parallel Diode Termination





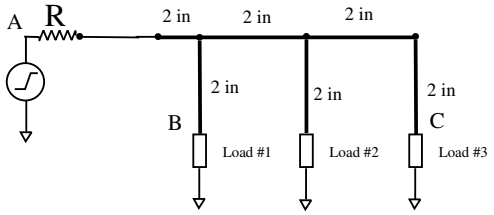
Parallel diode termination, risetime = 0.2 ns

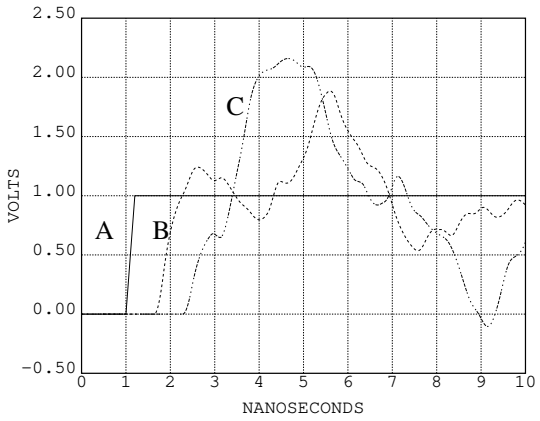


Parallel diode termination, risetime = 2 ns

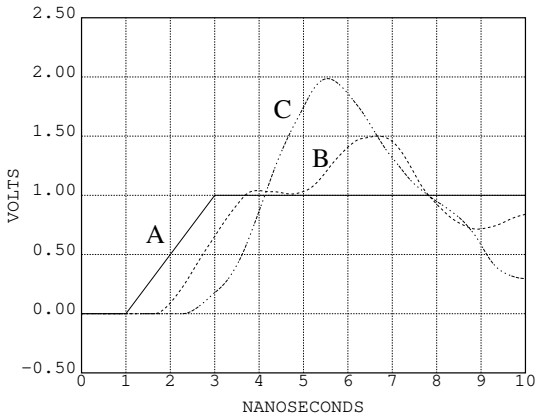
11.5.6 Multi-Branch (Long-Stub) Topology

Unterminated



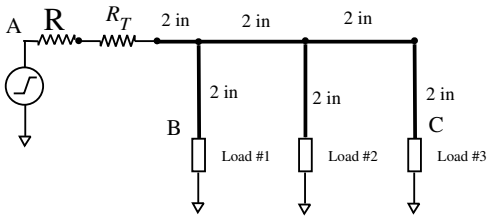


Unterminated, risetime = 0.2 ns

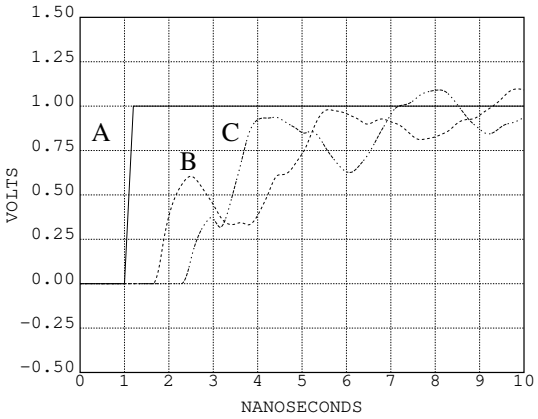


Unterminated, risetime = 2 ns

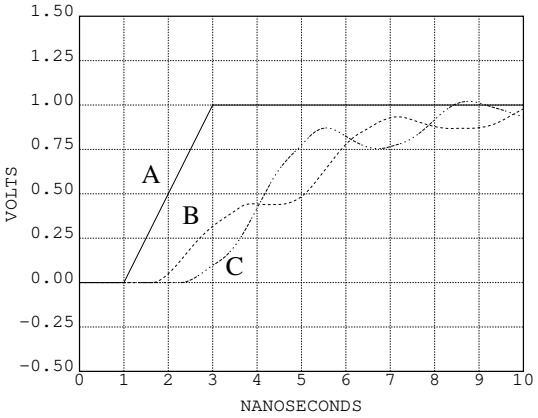
Series Termination



Note significant voltage division between (R_{dr}+R_T) and Z_o. Many reflections (and round-trips on line) required for signal to settle.

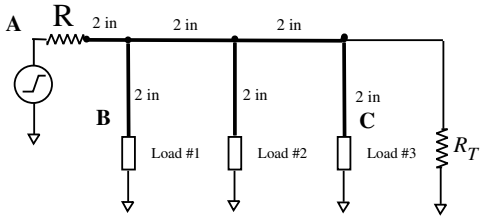


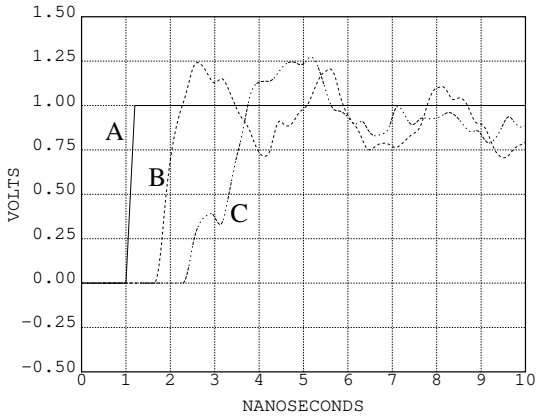
Series termination, risetime = 0.2 ns



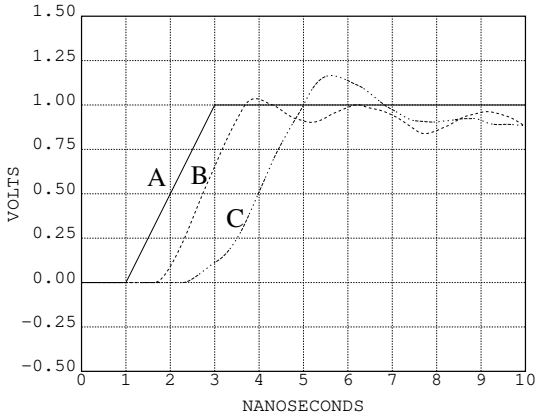
Series termination, risetime = 2 ns

Parallel DC Termination



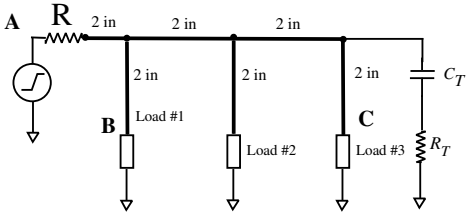


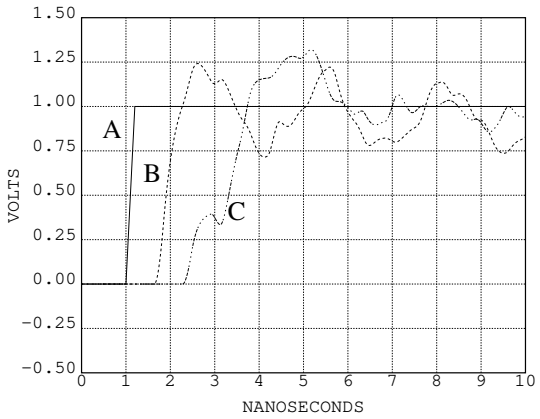
Parallel dc termination, risetime = 0.2 ns



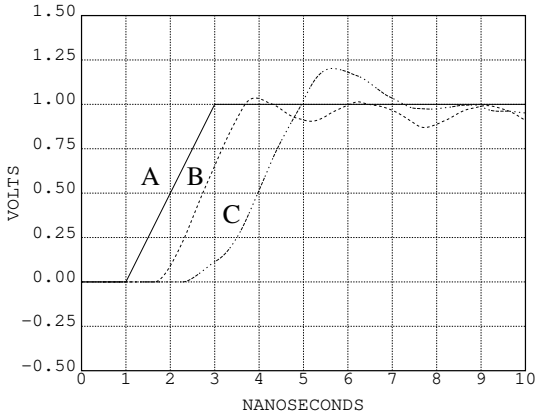
Parallel dc termination, risetime = 2 ns

Parallel AC Termination



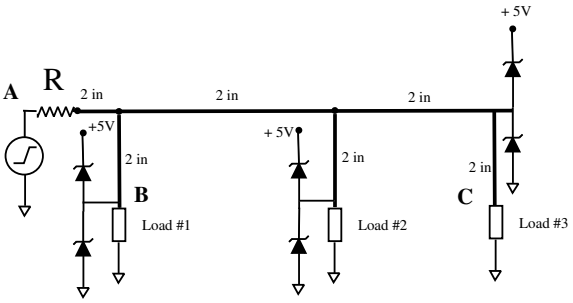


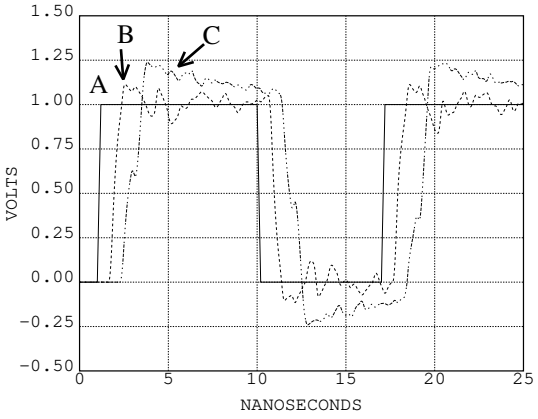
Parallel ac termination, risetime = 0.2 ns



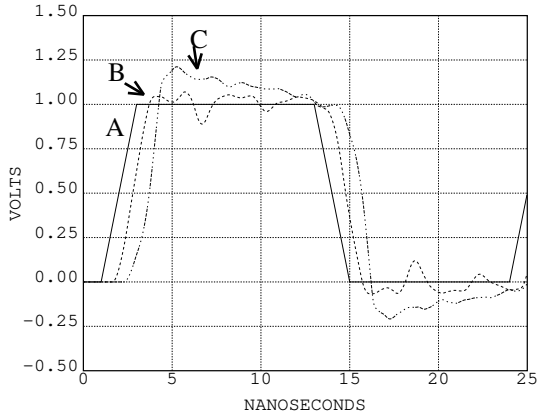
Parallel ac termination, risetime = 2 ns

Parallel Diode Termination





Parallel diode termination, risetime = 0.2 ns



Parallel diode termination, risetime = 2 ns

Appendix A: Referenced Documents

A.1 Digital EL-Class Documents

EL-00025-00	*DEC STD 025-0 Parts List*
EL-00030-02	*DEC STD 030-2 Module Manufacturing Standard - Product Safety Requirements*
EL-00030-04	*DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements*
EL-00030-05	*DEC STD 030-5 Module Manufacturing Standard - Module Assembly and Component Insertion Rules*
EL-00047-00	*DEC STD 047-0 Bar Code: Symbology Standard*
EL-00056-05	*DEC STD 056-5 Circuit Diagrams and Item Designations - Diagrams and Symbols*
EL-00100-05	*DEC STD 100-5 Engineering Change Orders - Financing ECOs to Harware*
EL-00102-00	*DEC STD 102-0 Environmental Standard for Computers and Peripherals - General Test Requirements*
EL-00105-00	*DEC STD 105-0 Display Workstation Ergonomics (Human Factors): Design Criteria*
EL-00176-04	*DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria*
EL-00184-00	*DEC STD 184-0 Programmable Integrated Circuit Documentation: Process and Requirements*
EL-EN432-00	*Archive Data Structure File Specification*
EL-EN654-00	*B Series Module Connector Detail and Circuit Outline (*Order EL-ENPCB-01*)*
EL-ENPCB-01	*PC Board Engineering Handbook - Standard Circuit and Finger Details*
EL-MF787-00	*Corporate Electronics - Packaging and Interconnect Strategy*
EL-MF777-00	*PLO File Specification, Version 3* (In process

A.2 Other Digital Documents

10-00001-GS	*Capacitors, Mylar, Fixed, Axial Lead*
10-00002-GS	*Capacitors, Tantalum, Quality/General Specification For*
10-00003-GS	*Capacitor, Mica, Dipped, General Specification For*
10-00100-GS	*Capacitors, Axial Leaded, Aluminum Electrolytic, General Specification For*
10-00101-GS	*Capacitor, Polarized Aluminum Electrilytic, P/C Mountable, Radial Leaded, General Specification For*
10-00102-GS	*Capacitor, Polarized Aluminum Electrolytic, Cylindrical, With Tapped Terminal Inserts, General Specification For*
10-00103-GS	*Capacitor, Ceramic, Monolithic, Axial Leaded, General Specification For*
10-00104-GS	Capacitor, Ceramic, Monolythic, Radial Leaded, General Specification For
10-00105-GS	*Chip Capacitor, Ceramic Dielectric, Multi-Layer, Unencapsulated, Leadless, General/Quality Specification For*

10-00106-GS	*Chip Capacitor, Tantalum, Dielectric, for General Purpose and High Frequency Types, General/Quality Specification For*
11-00001-GS	*General Procedure for Axial Lead Discrete Diodes*
11-00002-GS	*General Specification for DM Type Diode Assemblies*
11-00006-GS	*Diode, Switching, SOT23, General/Quality Specification For*
11-00007-GS	*Diode, Zener, SOT23, General/Quality Specification For*
11-00008-GS	*Diode, Schottky, Barrier, SOT23, General/Quality Specification For*
13-00013-GS	Resistors, Chip, Film, General Specifications For
15-00004-GS	*Transistor, SOT23, General/Quality Specification For*
18-05509-GS	*Oscillator, Crystal, Surface Mount, Plastic, General/Quality Specification For*
18-05507-GS	*Crystal, Oscillator, General/Quality Specification For*
19-00000-GS	*General Specification: Dimensional and Packaging Requirements for Multi-Package Dual-in-Line Packages*
19-00010-GS	*Array, Pin Grid Packages, Visual and Mechanical, General Specification For*
19-00013-GS	*Plastic Leaded Chip Carriers, General Specification For*
19-00015-GS	*Array, Gird, Packages, General Specification For*
19-00017-GS	*Packages, Small Outline (SOP), and Small Outline - Large (SOL), Integrated Circuit, General Specifications for Plastic*
19-00019-GS	*Array, Pin Grid, Cavity Down, Ceramic Package, General Specification For*
19-00023-GS	*Quad Flatpacks, Plastic Molded, Metric Controlled Dimensions, General Specification For*
19-00031-GS	*Ceramic Quad, Flatpack Package Family, Ceramic Custom, With Top Brazed Leads, and Solder Sealed Lid, General Specification For*
19-00032-GS	*Leaded Chip Carriers, Plastic Packages, Small Outline J-Bend (SOJ), General Specification For*
19-00034-GS	*Packages, Cerquad Semiconductor, General Specification For*
19-00045-GS	*Shrink Small Outline Package (SSOP)*
19-00046-GS	*Thin Small Outline Package, General Specification for*
19-00048-GS	*Quad Flatpacks, Plastic Molded, Non-JEDEC Std., Metric Controlled Dimensions, General Specification For*
20-00001-GS	*Hybrid Circuits, Geneal Specification for Quality and Reliability Requirements*
21-00008-GS	*Dynamic Random Access Memories, General Specification for Packaging*
21-00019-GS	*Leaded Chip Carrier Semiconductor Packages, General Specification For*
EK-BASAA-FL	*Basic Introduction to WRL Tools*
EK-BATAA-FL	*Formats of DB Sort Input Files*
EK-BAUAA-FL	*Genrad Circuit Test File*
	SCO-SEG Packaging Technology and Design Guide

A.3 Documents External to Digital

IEEE 802.3	*Information Processing Systems - Local Area Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specification*
IPC 355	*Printed Board Automated Assembly Destription in Digital Form*
IPC 356	*Bare Board Electrical Test Information in Digital Form*
ISO 2110	*Information Technology - Data Communication 25 Pole DTE/DCE Interface Connector and Contact Number Assignments*
Mil-C-24308	*General Specification for Connectors, Electric, Rectangular, Miniature, Polarized Shell, Rack and Panel, Pin Contacts, Nonmagnetic, Class M and N, Solder Type*
Mil-P-13949	*General Specification for Plastic Sheet, Laminated, Metal Clad* (for Printed-Wiring Boards)

A.4 Order Information

Use VTX SMC to order copies of EL-class documents from Standards and Methods control. Send questions to JOKUR::SMC or call DTN: 234-4423.

General Purchase Specifications can be ordered from Central Specification Control Systems, Central Reproductions, DTN 223-2323, ECADJR::REPRO, or a Microfilm Reference File, or the SPOC System.

EK documents can be ordered from Publishing and Ciruclation Services, DTN 234-4325, NEST::ORDER.

EIA standards can be ordered from Electronic Industries Association, 2001 Pennsylvania Avenue, NW, Washington, DC 20006, Telephone (202)457-4900.

IEEE standards can be ordered from the Institute of Electrical and Electronic Engineers, Inc., 45 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855, Telephone 1-800-678-IEEE or (908) 562-3800.

IPC documents can be ordered from The Institute for Interconectig and Packaging Electronics Packaging, 3451 Church Street, Evanston, IL 60203, Telephone (313)677-2850.

ISO standards can be ordered from International Organization for Standardization, 3, rue de Varenbe, 1211 Geneve 20, Switzerland, Telephone +41 22 734 0150.

Military specifications can be ordered from Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120, Telephone (215) 697-3321.

A.5 Documents External to Digital

BPA System 2000, Advanced Interconnection and Substrates

IPC-T-50	*Terms and Definitions for Interconnecting and Packaging Electronic Circuits*
IPC-D-275	*Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies*
IPC-D-317	*Design Guidelines for Electronic Packaging Utilizing High Speed Techniques*
IPC-D-330	*Design Guide Manual*
IPC-D-335	*Electronic Packaging Manual*
IPC-A-600	*Acceptability of Printed Wiring Boards*
IPC-A-610	*Acceptability of Printed Wiring Board Assemblies*
IPC-R-700	*Suggested Guidelines for Modification, Rework, and Repair of Printed Boards and Assemblies*
IPC-CM-770	*Component Mounting Guidelines*
IPC-SM-780	*Component Mounting Guidelines, Surface Mount Technology*
IPC-SM-782	*Surface Mount Land Patterns*

High-Speed Board Design Techniques, AMD Publication Number 16356, 1992
Cypress Applications Handbook, 1989
TDR Fundamentals, HP Application Note 62, April 1988
Electromagnetic Fields and Waves, Paul Lorrain and Dale Corson, W. H. Freeman and Co., 1970, pp. 475-481.

A.6 Order Information

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send questions to JOKUR::SMC or call DTN: 234-4423.

Copies of Digital Internal Reports and Memos can be ordered from the contacts listed with each report.

IPC Standards can be ordered from The Institute for Interconnecting and Packaging Electronics Packaging, 3451 Church Street, Evanston, IL 60203, Telephone (313) 677-2850

BPA documents can be ordered from BPA (Technology & Management) Ltd., 50 Short Road, Cold Spring Harbor, NY 11724.

Appendix B: Related Documents

B.1 Digital EL-Class Documents

EL-00186-00	*DEC STD 186-0 Signal Integrity*
EL-SM030-00	D*EC STD 030 Module Manufacturing Standard*
EL-SM176-00	*DEC STD 176-0 Printed-Wiring Board Manual*
EL-SM140-00	*DEC STD 140 Documentation, Data, and Release Requirements for Printed-Wiring Boards, Modules and Backplanes*
EL-MF228-00	*Component Categories and Codes for Machine- and Non-Machine Insertable Components*
EL-ENPCB-01	*PC Board Engineering Handbook - Standard Circuit and FingerDetails*
EL-ENPCB-02	*PC Board Engineering Handbook - Layer Construction Drawings*
EL-ENPCD-TM	*Electrical Design Guide for Printed Circuits*
EL-MFPCB-04	*PC Manufacturing Handbook - Assembly Board Drawings*

B.2 Other Digital Documents

Analysis and Design of Interconnects with Coupled Lines, Colin Gordon, 14-Feb-1991.
Diode vs. Resistor Terminator on MAXVAX XL Clock Distribution, Kevin Roselle and Tom Wenners, 1-May-1989.
Modal Solution of Multiconductor Transmission Lines, Colin Gordon, 24-Apr-1989.
On-chip Capacitance vs. Package Capacitors, Design Tradeoffs for Reducing Simultaneous
Physical Limitations of Backplane Busses on Signal Integrity, Michael Tsuk 24-May-1991.
RIGEL Clock, Diode Termination, Don Vonada, 12-Feb -987.
Switching Noise in CMOS, Judy Chen, 13 May-1991.
The Effects of Losses on Signals in PWBs, Rich Evans, 21-Jan-1992.